Ultra-Scaled III-V XOI FETs For Next Generation Logic Application

by

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Declaration

This is to certify that the thesis work entitled **"Ultra-Scaled III-V XOI FETs For Next Generation Logic Application"** has been carried out by Md. Nur Kutubul Alam in the Department of Electrical and Electronic Engineering, Khulna University of Engineering & Technology, Khulna, Bangladesh. The above thesis work or any part of this work has not been submitted anywhere for the award of any degree or diploma.

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Abstract

Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are the heart of microelectronic industries and found its application in almost every device from microprocessor, memory to communication electronic devices. In the quest of high packing density, improved performance, and low power consumption, size of MOSFETs are being reduced for last four decades, and now it is approaching to its physical limits. Addressing to this issue, a novel "XOI FET" was proposed previously in order to continue the scaling as well to lower the power consumption. But the XOI FET itself has to face some key challenges to penetrate the electronic industry. In this research we address to each of the challenges associated with the materialization of XOI FET and proposed their solution. Comparing the logic figure of merits, it is found that thinner channel (3nm) XOI FET gives better result than thicker one. At thinner channel, interface properties of XOI FET play a critical role, however their impact can be compensated. To study the quality of the interface, ideal Capacitance-Voltage characteristics are reported that shows an anomalous staircase nature. It is also reported that the XOI FET having InGaSb channel material outperforms the InAsSb. From fabrication point of view, prospect of junction less XOI FET for next generation logic devices is also presented.

Acknowledgements

Contents

List of Figures

List of Tables

Abbreviations

MOSFET -Metal-Oxide-Semiconductor Field-Effect-Transistor

SOI -Silicon on Insulator

XOI -Anything on Insulator in general. In this thesis, III-V on insulator

JLXOI -Junction Less XOI

C_{ox} -Oxide Capacitance

DGMOS -Double Gate MOS

MS -Mode space

UMS -Uncoupled Mode Space

CMS -Coupled Mode space

ITRS -International Technology Roadmap for Semiconductor

TB -Tight Binding

EF -Fermi Energy

EOT -Equivalent Oxide Thickness

UTB -Ultra-thin-body

WF -Work Function

CBM -Conduction band minima

VBM -Valence band minima

CNL -Charge neutrality level

TOB -Top of the barrier

Dedicated to my beloved Parents...

Chapter 1

Introduction

Chapter Outlines

- Introduction

- Objectives of the thesis work

- Layout of the thesis work

1.1 Introduction

The Si based metal-oxide-semiconductor field-effect-transistors (MOSFETs) are the heart of modern microelectronic industries. It is nothing but a switch which controls the flow of current from source to drain using gate that acts as a valve. Owing to mature and low cost fabrication facility, Si MOSFETs with SiO_2 gate-dielectric are being widely used almost everywhere from microprocessor, memory chips, and telecommunication micro-circuits [1,2,3]. In most of the cases MOSFETs are mainly used for logic operation, although it can serve other purposes. To meet the demand of high speed and high performance electronic devices in future, the main interest is to make them in such a way that they will work at ultra high speed with very low power dissipation. However, to achieve these goals, the reduction of transistor size is the only pathway. Scaling of the dimensions of transistors has led to exponential increase in density and switching speed, and a similar decrease in the switching energy [4]. Miniaturizing the MOSFETs allows the integration of more transistors in a single chip that results decrease in manufacturing cost of integrated circuits. The reduction of cost dramatically improved the manufacturing capabilities as well as reduced the line of width year by year. Observing the trend, Gordon Moore predicted that the density of transistor on a chip would double in every 18 months [5]. It is the famous prediction known as Moores law.

1.1.1 Scaling issues in MOSFET

While transistor size has been scaling down continuously following the Moores law, the basic structure of the MOSFETs remains unchanged until they showed some critical problems [6,7]. As the number of transistors per chip increased exponentially, the processor power continued to rise even with scaling the supply voltage due to increased die size and fast frequency scaling [8]. When the total power dissipating in the microprocessor reached 100W (FIG. 1.1), the frequency and die scaling were stopped. MOSFETs entered a power constrained scaling phase where the power dissipation was limited to 100W per chip [9]. To integrate more functions or to pack more transistors into the microprocessor, the supply voltage was required to be scaled. Since the threshold voltage and the sub-threshold slope of the

transistor did not scale with the supply voltage [11], the leakage power density continued to increase as the supply voltage was scaled. Scaling the supply voltage without scaling the threshold voltage would lead to reduced switching speed and slower performance, which is not desired. However, near threshold voltage operation can improve the energy efficiency of computing as shown in FIG. 1.2, and can help scale the supply voltage [12]. Beside the problem of power consumption, when the gate length (L) of a device become less than 100 nm, it suffers from various adverse effects including short channel and hot electron effects, parasitic capacitance, leakage current, transistor isolation etc. Moreover, velocity saturation [13] and source velocity
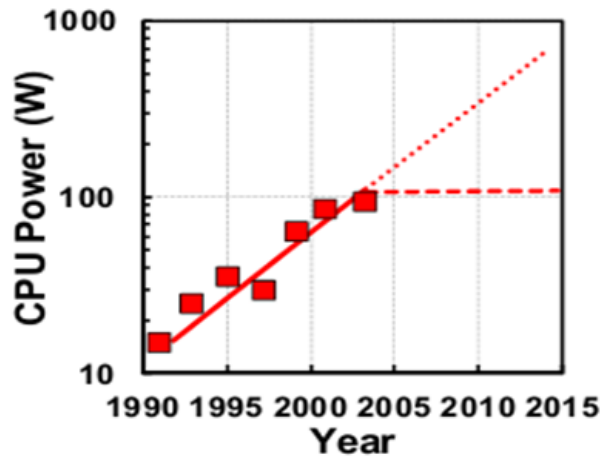
FIGURE 1.1: Power dissipation in CPU for various technologies as a function of the year of introduction (Source: [10]).

limit [14] blocks the further performance improvement of Si MOSFETs. To solve these problems researchers tried several approaches including strain engineering [15]. But it is observed afterward that the traditional bulk Si MOS structure has to be changed to compensate the problems. Replacement of bulk silicon (Si) substrate with silicon-on-insulator (SOI) did drastically improve the device performance by suppressing these adverse effects [16,17]. The successful suppression of the short channel effect (SCE) allowed the scaling to continue. However, while the gate length of SOI FET is scaled down, the area of gate oxide as well as the oxide-capacitance (Cox) is reduced.

To keep control over the channel, a certain level of Cox is mandatory. Therefore, to keep that minimum Cox the oxide thickness was also reduced. But such scaling of gate dielectric also has a problem. When the physical thickness of SiO_2, which is the mostly used dielectric in Si
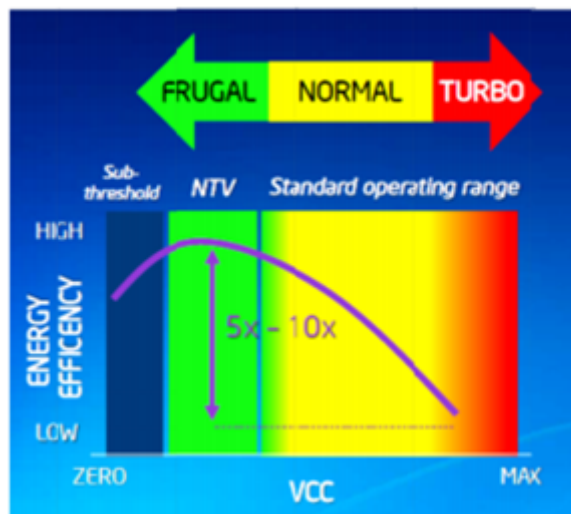
FIGURE 1.2: Transistor operating voltage range showing energy efficient computation for near threshold voltage operation. (Source: [10] Intel Labs ISSCC .

MOSFETs, goes below 1.2 nm, the quantum mechanical tunneling becomes significant [18,19]. Any further scaling of gate oxide would increase the static gate leakage and lead to significant power consumption at the off state of the device. The solution to this problem is to use a gate dielectric having higher dielectric constant, known as high-k dielectric. The high-k dielectrics can be grown physically thicker than the SiO_2 that will give the same oxide capacitance. The physical thickness of SiO_2 required for giving the same Cox, if it were used in the place of high-k dielectric is known as the Equivalent oxide thickness or EOT of that high-k material [19]. However, up to 45 nm gate length, use of high-k material as a gate dielectric in SOI FETs has been a successful solution, but it is not enough for further scaling [20]. At this stage, leaving the planner technology and adopting the multi-gate structure, like Double-Gate-MOSFET (DGMOS), tri-gate-FinFET etc. were thought to be the solution [21,22,23]. In the multi-gate FET, the channel is controlled electrostatically by the gates from multiple side of the channel. It offers better control over the channel with a reduced gate leakage current. Improved gate control also offers lower output conductance, i,e smaller $(dI_d)/(dV_d)$ at saturation region and improved on state current (I_{ON}) for several reasons [24]. Moreover, the lowest subthreshold slope (SS) to date is also reported for tri-gate SOI FET which is 63 mV/dec [25]. Therefore, from the expectation of more possibilities, several FinFET technologies and their advantages are demonstrated in [26,27,28,29] in details. Utilizing these technological innovations (high-metal gate, strain and tri-gate architectures), transistors with improved performance have been fabricated that operate at a moderate supply voltage (from 1.2V for planar 65nm SOI to 0.9V for 22 nm tri-gate transistors) [10,1]. However, adopting the multi-gate technology is not simple as well as straight forward. The main disadvantage of multi-gate architecture is its 3D construction. Fabrication of such 3D devices is challenging and costly in comparison with planner technology [30,31,32,33,34,35,36]. Moreover, in contrast, the planer SOI has a back gate connected to their substrate. While process induced fluctuation of threshold voltage (V_{th}) is very common [37], the threshold voltage of such device can be controlled by applying bias at the back gate. Even, this feature can be used to dynamically raise or lower Vth circuit by circuit within a chip in response to the need for less leakage or more speed. This is a very effective means of managing power consumption [20]. Considering all these facts of simple low cost manufacturing as well as robust controllability, the SOI (or any advanced version of it) would still be the best option; if the adverse effects of scaling of SOI FETs can be overcome.

1.1.2 Advent of XOI FET

To overcome the scaling challenges of SOI, replacement of Si from the channel with a material having better electron transport properties could be one of the ways. Group III-V compound semiconductors exhibit outstanding electronic and optical properties, including high electron mobility and high peak saturation velocity [38], due to their small effective mass in the valley. The comparison of electron and hole mobilities of different III-V materials is shown in fig. 1.3 [4].

Use of III-V materials at the channel would allow reduction in operating voltage without compromising the switching speed and thereby reduces the power consumption. Further downscaling may be feasible [39]. Additionally, III-V semiconductors have a mature and large industry for solid-state lighting and transceivers for optical communications [40]. Therefore, integration of III-V semiconductors on Si platform could be the royal road for achieving high performance miniaturized devices at low power consumption. With that aim, in analogy to SOI, n-type InAs FETs were experimentally demonstrated on Si/SiO_2 substrate [41] and the structure is termed as XOI to represent compound semiconductor-on-insulator platform. Due to similar device structure, XOI also offers all the advantages of SOI. Therefore, the suppression of SCE makes the XOI a promising technology for sub-100-nm node and beyond [42].

1.1.3 Challenges of XOI FET

While XOI promises to offer better device performance than SOI, several critical challenges need to be addressed to penetrate the global semiconductor industry. One of the main challenges of XOI is to optimize the interfacial (i.e., gate oxide-channel, channel-buried oxide and buried oxide-substrate) charge properties. In order to utilize the excellent transport properties of III-V, the interface properties need to be improved. For better control and high I_{ON}/I_{OFF} ratio, the channel thickness needs to be reduced significantly. However, with continuous reduction in channel thickness, the interface charge properties start to dominate the device performance [43,44]. Further, interface traps close to or beyond the conduction band edge can alter the carrier density and transport properties [45]. However, challenges of the growth of XOI FET
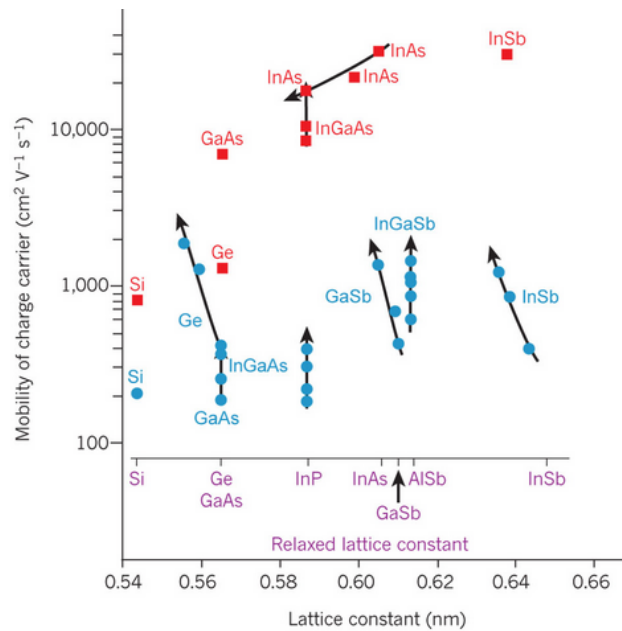
FIGURE 1.3: Electron and hole mobilities of various III-V compound semiconductors (Source: del Alamo MIT [4]). Antimonidesare very attractive since they have high electron as well as high hole mobility.

maintaining reasonable interface quality has been overcome by Ali Javey et. al. [46]. Nevertheless, the quality of interface after growth should be checked by detail CV measurement. The channel thickness also has a great impact on the mobility. The electron-phonon scattering and phonon limited mobility degradation becomes prominent for very thin channel [47]. This is recently demonstrated in InAs XOI, wherein the mobility of InAs XOI was strongly dependent on channel thickness [48]. The study has been carried out at 200 nm gate length; however, to best our knowledge, performance of XOI FET at sub-20 nm regime has not been comprehensively studied. At this ultra-scaled limit, electronic transport becomes ballistic and therefore concept of mobility does not work. That is why, the thickness dependent mobility degradation is not a problem. But keeping the control of gate over the channel, especially at planner architecture is still a challenge.

1.2   Objectives of the thesis work

In recent years researches on XOI FET are becoming very much attractive due to its enormous prospect in ultra-scaled and ultra-low-power logic devices. Among the III-V semiconductor materials InGaSb based XOI nFET is expected to be suitable for high-speed and low power logic devices. The main objectives of this thesis work are to propose a ultra-thin-body InGaSb based XOI nFET device structure and then mathematically model as well as numerically simulate the device performance. The research work is performed based on the following targets-

- To study the channel thickness dependent I-V characteristics

- To study the impact of interface states on I-V characteristics

- To identify the suitable channel material

- To study the the effect of different high-k gate oxide

- To study the prospect of Junctionless XOI FET

- To study the CV characteristics as a function of different process parameters

1.3   Layout of the thesis work

In **Chapter 2**, starts with the need of numerical simulation of semiconductor devices to analyze the performance of devices in quantum regime. Non equilibrium Greens function (NEGF) is widely used in nanoscale devices to measure the transport characteristics. Usually there are two types of approach for the solution of NEGF equation; we are using mode space (MS) approach for pure quantum mechanical treatment of XOI nFET. Mathematical formulation along with the solution are discussed for the MS approach. Also the device structure and material parameters used in this study are summarized in this chapter.

In **chapter 3**, presents the result and discussion obtained from the analysis of the XOI nFET. Firstly the ballistic I-V characteristics are studied using NEGF theory. Channel material-dependent and channel thickness-dependent performance of the XOI nFET are discussed. Then the capacitance voltage characteristics of the device is studied as a function of several physical and process parameters. Then the effect of different gate oxide having same EOT is studied. Finally Comparison of the performance between traditional n-i-n channel vs junctionless channel is presented.

Finally, in **chapter 4**, the concluding remarks and recommendation for future work is presente.

Chapter 2

Device Structure, Physics, and Mathematical Modeling

Chapter Outlines

- Introduction

- Structure of XOI device

- Physical and material parameters

- Energy of electron in conduction

- Mathematical Modeling of IV Characteristics

  - Ballistic transport theory

  - NEGF Formulation

  - Quantum Transport Simulation Using Mode Space Approach

- Mathematical Modeling for Capacitance-voltage (CV) Characteristics

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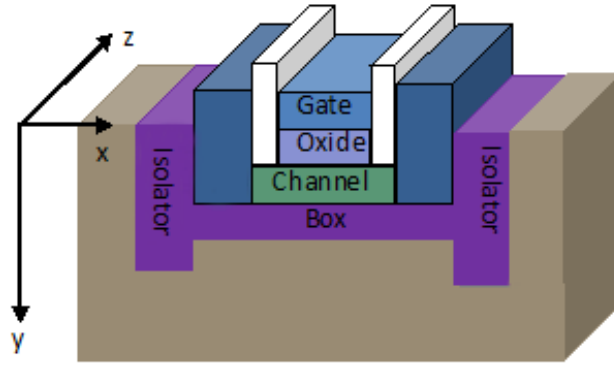
FIGURE 2.1: Structure of the XOI nFET device under study.

2.1 Introduction

Device modeling and numerical simulation is very much important to optimize the parameters and hence to perform the experiment. The prediction of device behavior before fabrication is the most advantageous feature of device simulation over experimental measurement. Running a computer based simulation is cost effective in comparison with fabrication and performing different types of measurements. Device simulation allows to set up different conditions (under which fabricated device may be damaged) to be tested inexpensively. Moreover, it is possible to simulate devices which arent yet manufactureable.

2.2 XOI device structure

FIG. 2.1 shows the physical structure of the XOI nFET under study. In this figure x is the transport direction, y is the confinement direction and z is the direction along the width of the device. All relevant parameters used in device simulation are listed in Table 2.1.

Parameter name	Value	Description
ϵ_{ins}	22	HfO_2 as gate oxide
t_{body}	3 nm	Channel thickness in general.
		(Special cases are specified in proper place)
t_{ins}	2.82 nm	Thickness of gate oxide.
		[Equivalent Oxide Thickness (EOT)=0.5 nm]
L_G	15 nm	Gate length (Region right below gate oxide)
L_{SD}	5 nm	Extension of channel toward Source/Drain
N_{Body}	p-type 10^{15}/cc	Doping at channel region
N_{SD}	n-type 10^{20}/cc	Doping at L_{SD} region

TABLE 2.1: The physical and material parameters of the XOI nFET. Device structure is shown in FIG. 2.1.

2.3   Energy of electron in conduction

Dynamics of an electron in any system is described by time dependent Schrodinger equation. But for a bounded system, from which electron cannot escape, the electronic wave function becomes stationary. This stationary wave functions can be described by the time independent Schrodinger equation. In one dimension, it can e expressed by-

$$-\frac{\hbar^2}{2m}\frac{d^2\psi}{dx^2} + V\psi = E\psi \tag{2.1}$$

Where, V is the potential energy of electron and E is the total energy. Now, let the solution of this equation is,

$$\psi = Ae^{ikx} \tag{2.2}$$

After second derivative of ψ with respect to x and then substitute into equation 2.1, we get

$$-\frac{\hbar^2}{2m}(-k^2 Ae^{ikx}) + V Ae^{ikx} = EAe^{ikx} \tag{2.3}$$

or

$$E = V + \frac{\hbar^2 k^2}{2m} \tag{2.4}$$

Equation 2.4 is called the dispersion relation for Schrodinger equation. Here, V is the potential energy and E is the total energy, the second term of equation 2.4 must be the kinetic energy. Also notice in equation 2.4 that E depends on the wave vector k, and it shows a parabolic relation with k. The Schrodinger equation and the dispersion relation can be extended to 3D as follows-

$$-\frac{\hbar^2}{2}\left(\frac{\partial^2}{m_x\partial x^2} + \frac{\partial^2}{m_y\partial y^2} + \frac{\partial^2}{m_z\partial z^2}\right)\psi\,(x,y,z) + V\psi\,(x,y,z) = E\psi(x,y,z) \tag{2.5}$$

$$E = V + \frac{\hbar^2 k_x^2}{2m_x} + \frac{\hbar^2 k_y^2}{2m_y} + \frac{\hbar^2 k_z^2}{2m_z} \tag{2.6}$$

While dealing with a particular material, m_i (i = x, y or z) must be replaced by the effective mass m_i^*. However, to sustain a stationary wave inside a bounded system, only some specific wave lengths associated with specific wave vectors and energy eigen states are allowed. Occupation of those energy levels determines the charge dynamics inside a system. From that charge dynamics, both capacitance-voltage and transport behavior are measured.
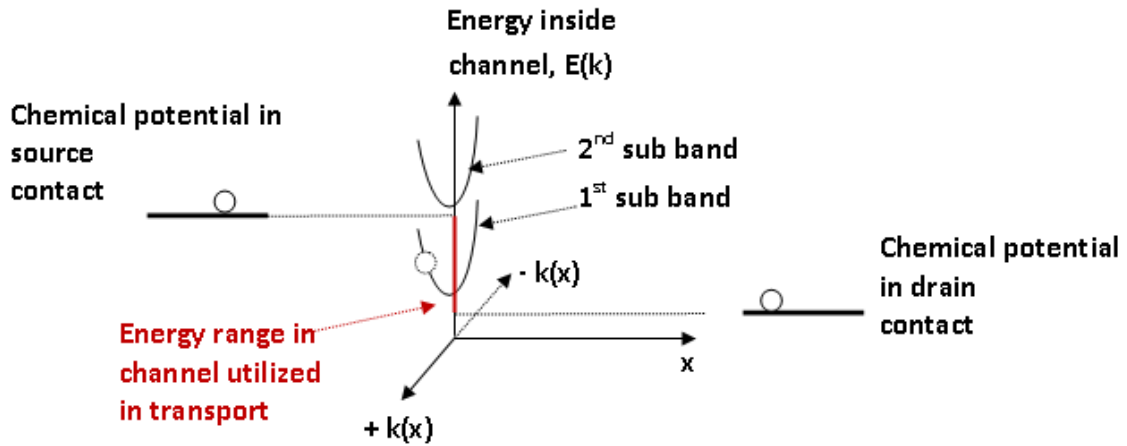
FIGURE 2.2: Carrier transport mechanism inside a ballistic MOSFET.

2.4 Mathematical Modeling of IV Characteristics

2.4.1 Ballistic transport theory

Relation of energy of an electron inside a system is explained in section 2.3, by equation 2.4. When the system is large (bulk material), the energy become continuous and electron resembles to a classical particle. But if dimension of the system gets very low, for example in case of XOI FET, the diemnsion of channel along y axis is few nano meter, then allowed energy levels of electron are discretized and they form several groups. Each of the group is called subbands. And each subbands contains some allowed energies of electron. But there is no allowed energy levels in between two subband. Typical sub bands in the channel of XOI nFET as a function of wave vecor k is shown in centre part of Fig. 2.2. Here positive k indicates the electron wave is travelling along positive x axis and negative k means the opposite. However, sicne energy does not depend on the direction of travelling, the curve of subbands is symmetric in positive and negative k axis.

Electrons inside the source contact possess an energy identified by the chemical potential in it, which is given by the Fermi level at the source contact. When the electrons find some energy levels inside the channel which are below their chemical potential, they try to occupy that lower level and therefore moves to the channel. Since electron travels to positive x direction, it occupies one of the +k states of 1st subband shown in Fig. 2.2. It did not occupy the 2nd subband because that lies at a higher energy. After that, if the incoming electrons find the chemical potential of the drain contact which is located at a further lower energy, they move toward the drain contact. By this mechanism, electrons move from the source to drain through the channel, provided that, allowed energy levels inside the channel are located anywhere in between the chemical potential of the source and the drain contact (red marked portion of the energy axis in Fig. 2.2). The difference of the chemical potential between source and drain can be created by applying drain bias. And the position of subband is moved up or down

by applying gate bias. The amount of carrier flow depends on the number of energy states inside the channel located in between the two chemical potentials. Because according to Paulis exclusion principle, each energy level can be occupied by two oppositely spinning electrons. So, increase in the number of energy levels in the channel leads to increase in the number of travelling electrons. Since the current is defined as the charge transfered per unit time, the total current through the channel depends therefore on the amount of moving carrier, i,e the number of energy states in the channel, and on the speed at which electrons are moving [49]. At channel length less than 100 nm, carrier transport is practically ballistic. They face almost no scattering and therefore concept of mobility does not hold here. That is why, the speed of carrier is expressed by injection velocity, which is determined by the band structure of the channel alone. Considering all of these facts together, there is a well established mathematical formalism derived from the basic laws of quantum mechanics, namely Non Equilibrium Greens Function or NEGF. In case of coherent and non coherent transport, electron-electron interaction and all other quantum mechanical phenomena is therefore embedded in this model.

2.4.2 NEGF Formulation

The NEGF provides a rigorous description of quantum transport in nano-scale devices. For ballistic transport, NEGF is equivalent to solving Schrdinger equation for a semi-open system. The NEGF, however, provides a powerful way for treating the boundary of 2D and 3D problems. Moreover, it provides a way for treating scattering within non-ballistic devices. The rigorous description for this formalism can be found in the literature [50,51,52,53,54,55,56,57,58,59] where it is described using an advanced language in the quantum mechanics world, namely, the second quantization language. A simpler description can be found also in the literature [60,61,49,62].

2.4.3 Quantum Transport Simulation Using Mode Space Approach

Quantum Transport involves solution of Schrodinger equation using open boundary condition at points where electrons comes into or leave form the region (device) under study. As electric field is invariant along the width of XOI FET (z direction in FIG. 2.1),the Schrodinger equation can be solved at a slice taken perpendicular to the "z" direction, i.e. x-y plane. 2D Schrodinger equation at the x-y plane is given by-

$$-\frac{\hbar^2}{2}\left(\frac{\partial^2}{m_x\partial x^2}+\frac{\partial^2}{m_y\partial y^2}\right)\psi\left(x,y\right)+V\psi\left(x,y\right)=E\psi(x,y) \qquad (2.7)$$

It can be solved in real space (RS) or mode space (MS) approach. Computational efficiency is needed to make the self-consistent approach suitable for device design and characteristics prediction. The NEGF method has the advantage of being rigorous but the disadvantage of being heavy in computations [63]. Real-space (RS) representation is the most accurate, yet

complex, representation used in the NEGF [64]. For nano-scale transistors, it is more convenient, to solve Schrdinger equation in the mode-space (MS) [65,66] where computational burden is affordable. The uncoupled mode-space (UMS) provides enormous saving in the computational burden but suffers from being valid only for ultra-thin body double-gate (DG) MOSFET [63]. In contrast, the coupled mode-space (CMS) can be used for either thin or thick bodies but its computational cost is more than the UMS. In this chapter we review the MS approach and examine the validity of the UMS. Moreover, the possibility of reducing the CMS computations is examined. In the NEGF framework, a suitable set of basis function is chosen in terms of which the operators like the Hamiltonian operator and the Greens function are represented. The MS approach is based on the assumption that the active device is decoupled from the gate contacts [64]. Decoupling is achieved by applying closed boundary condition at the insulator-metal interface. It may be also applied at the semiconductor-insulator interface if the conduction band offset between the semiconductor and the insulator is taken to be infinite. Applying the closed boundary condition at whether of the two interfaces gives rise to subbands or modes. The subbands are the eigenfunctions associated with the confinement in the gate confinement direction (y-direction in FIG 2.1). The XOI FET is given in Fig. 2.3 where it is divided into vertical slices with Δx spacing in the x- direction. The subbands of the structure are obtained by solving a 1D Schrodinger equation in the y direction with each vertical slice, positioned at x=x$^{/}$, along the x direction. For n$^{\text{th}}$ subband, it is given by-

$$-\frac{\hbar^2}{2m_y^*}\frac{\partial^2\chi^{(n)}\left(x^{'},y\right)}{\partial y^2} + +E_c\left(x^{'},y\right)\chi^{(n)}\left(x^{'},y\right) = E^{(n)}\left(x^{'}\right)\chi^{(n)}\left(x^{'},y\right) \tag{2.8}$$

Where $\chi^{(n)}$(x$^{/}$, y) is the eigenfunction in the y-direction at x=x$^{/}$ and E(n)(x$^{/}$) represents the bottom of the subband at x$^{/}$ and n is the subband index.

At each vertical slice x$^{/}$, the central difference approximation for the second derivative of $\chi^{(n)}$ is applied:

$$\frac{\partial^2\chi_j^{(n)}}{\partial y^2} = \frac{\chi_{j+1}^{(n)} - 2\chi_j^n + \chi_j^{(n)}}{\left(\Delta y\right)^2} \tag{2.9}$$

where $\chi_j^{(n)}=\chi^{(n)}$ (x$^{/}$,y_j) Substituting equation 2.9 into equation 2.8, we obtain:

$$-t_y\chi_{j-1}^{(n)} + 2t_y\chi_j^{(n)} - t_y\chi_{j+1}^{(n)} + E_c\chi_j^{(n)} = E^{(n)}\chi_j^{(n)} \tag{2.10}$$

Using equation 2.10 for each node along the vertical slice x$^{/}$ and then applying closed boundary condition at the semiconductor insulator interface, as set of linear equation are obtained and cast in the matrix form:
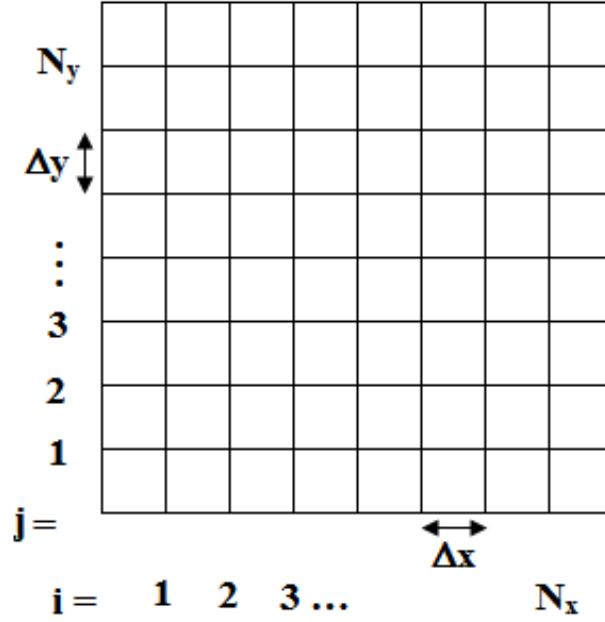
FIGURE 2.3: A model of any geometric space divided into vertical slices. The horizontal spacing between the slices is Δx. The same is used in discretization of the XOI FET.

$$\begin{bmatrix} 2t_y + E_{c1} & -t_y & 0 & 0 & \cdots & 0 & 0 & 0 \\ -t_y & 2t_y + E_{c2} & -t_y & 0 & \cdots & \cdots & 0 & 0 \\ 0 & -t_y & 2t_y + E_{c3} & -t_y & \cdots & \cdots & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & & & \vdots & \vdots \\ 0 & \vdots & \vdots & & \ddots & & \vdots & \vdots \\ 0 & 0 & \vdots & & & \ddots & & \vdots \\ 0 & 0 & 0 & 0 & \cdots & -t_y & 2t_y + E_{c3} & -t_y \\ 0 & 0 & 0 & 0 & \cdots & 0 & -t_y & 2t_y + E_{cN_y} \end{bmatrix} \begin{bmatrix} x_1^{(n)} \\ x_2^{(n)} \\ \vdots \\ \vdots \\ \vdots \\ x_{N_y}^{(n)} \end{bmatrix} = E^{(n)} \begin{bmatrix} x_1^{(n)} \\ x_2^{(n)} \\ \vdots \\ \vdots \\ \vdots \\ x_{N_y}^{(n)} \end{bmatrix}$$

$$(2.11)$$

Equation 2.11 is an eigenvalue problem that can be solved for different subbands. Each subband has an eigen energy $E^{(n)}$ and corresponding eigenvector $\chi^{(n)}$ within each slice positioned at x$^/$ along x direction. Only the lowest N_m subbands are considered and rest are ignored due to their high subband energies $E^{(n)}$ and consequently low occupation probability. The essence of the MS representation is the expansion of the 2D wave function ψ(x,y) of the equation 2.7 in terms of subbands in the form:

$$\psi\ (x,y) = \sum_{n=1}^{n=N_m} \phi^{(n)}(x)\chi^{(n)}(x,y) \tag{2.12}$$

where $\phi^{(n)}$(x) are the expansion coefficients. As indicated in the previous paragraph, only few subbands are taken into consideration and, as a result, the summation is truncated at n= N_m

. Substituting equation 2.12 into 2D Schrodinger equation, multiplying by $\chi^{*(m)}$(x,y) and then integrating over y gives [67] :

$$-\frac{\hbar^2}{2m_x^*}\frac{\partial^2\phi^{(m)}(x)}{\partial x^2} + [E^m(x) - E_l]\phi^m(x) = \sum_{n=1}^{n=N_m} A_{mn}\phi^{(n)}(x) \tag{2.13}$$

where A_{mn}(x) is the operator given by:

$$A_{mn}(x) = \frac{\hbar^2}{2m_x^*}\left[2\int dy\chi^{*(m)}(x,y)\frac{\partial}{\partial x}\chi^{(n)}(x,y)\frac{\partial}{\partial x} + \int dy\chi^{*(m)}(x,y)\frac{\partial^2}{\partial x^2}\chi^{(n)}(x,y)\right] \tag{2.14}$$

Equation 2.13 is the CMS transformation of real space approach. For each node m, the right hand side involves a summation over all other modes and the m_{th} mode itself. This summation gives rise to coupling between the modes. The channel of ultra-thin body XOI FET is fully depleted and the shape of the potential E_c(x,y) along the y-direction varies slowly with x-position, hence the variation of χ with x can be neglected and equation 2.13 becomes

$$-\frac{\hbar^2}{2m_x^*}\frac{\partial^2\phi^{(m)}(x)}{\partial x^2} + E^{(m)}(x)\phi^{(m)}(x) = E_l\phi^m(x) \tag{2.15}$$

Equation 2.15 is called the uncoupled mode-space transformation of real space solution of the NEGF equation. The equation 2.15 also represents the 1D transport model equation that will be solved using the NEGF for each subband m. This Schrodinger like equation and can be expressed as-

$$H_m\phi^{(m)} = E_l I\phi^{(m)} \tag{2.16}$$

where

$$H_m = -\frac{\hbar^2}{2m_x^*}\frac{\partial^2}{\partial x^2} + E^{(m)} \tag{2.17}$$

For ballistic transport, this equation is to be solved using open boundary condition. Within the NEGF framework, the correct (open) boundary condition is incorporated through the use of the drain and source self- energies $\Sigma^{D(m)}$ and $\Sigma^{S(m)}$ respectively for each mode m [65]. Then the mth mode retarded Greens function G_m is given by:

$$G_m = [EI - H_m - \Sigma_s^m - \Sigma_D^m]^{-1} \tag{2.18}$$

The open boundary condition (for m$^{\text{th}}$ mode) is applied by setting $\phi_0 = \phi_1 e^{-ik_1\Delta x}$ and ϕ_{Nx+1} $= \phi_{Nx} e^{ik_{Nx}\Delta x}$, where $E_l = E_1{}^m + 2t_x(1\text{-}\cos(K_1\Delta x)) = E_{Nx}{}^m + 2t_x(1\text{-}\cos(K_{Nx}\Delta x))$ is the E-K dispersion relation in the source and drain contact. Then the source and drain self energy matrics for m$^{\text{th}}$ mode are given by-

$$\Sigma_D^m = \begin{bmatrix} 0 & .. & & 0 \\ .. & .. & & .. \\ 0 & .. & -t_x e^{ik_{Nx}x} \end{bmatrix}_{Nx \times Nx} \tag{2.19}$$

$$\Sigma_S^m = \begin{bmatrix} -t_x e^{ik_{N1}x} & .. & 0 \\ .. & & .. & .. \\ 0 & .. & 0 \end{bmatrix}_{Nx \times Nx} \tag{2.20}$$

After that the m$^{\text{th}}$ mode broadening functions Γ_S and Γ_S are obtained by-

$$\Gamma_s^m = i[\Sigma_s^m - \Sigma_s^{+m}] \tag{2.21}$$

$$\Gamma_D^m = i[\Sigma_D^m - \Sigma_D^{+m}] \tag{2.22}$$

Afterward the m$^{\text{th}}$ mode spectral density functions are obtained from broadening function and retarded Greens function as-

$$A_s^{(m)} = G^m \Gamma_s G^{m+} \tag{2.23}$$

$$A_D^{(m)} = G^m \Gamma_D G^{m+} \tag{2.24}$$

Then the m$^{\text{th}}$ mode longitudinal energy resoled electron density at a gird point i (along x) is obtained by-

$$n(i, E_l) = \frac{1}{2\pi\Delta x}[A_S F(E_l - E_{fs}) + A_D F(E_l - E_{fD})] \tag{2.25}$$

The net 2D electron density at i$^{\text{th}}$ node n(i) is obtained by integrating over E_l. This 2D electron density can be transformed into n(i,j) by-

$$n(i, j) = \frac{1}{\Delta y} n(i, E_l) \chi |(i, j)|^2 \tag{2.26}$$

Then the m$^{\text{th}}$ mode transmission coefficient from the source contact to the drain contact is defined in terms of the Greens function and the broadening function as-

$$T_{SD}^{(m)} = Trace[\Gamma_s{}^{(m)} G^{(m)} \Gamma_D{}^{(m)} G^{+(m)}] \tag{2.27}$$

And the m$^{\text{th}}$ mode longitudinal energy resolved terminal current is given by- Total current can be obtained by integrating over E_l.

$$I^m\left(E_l\right) = \frac{q}{2\pi h}T_{SD}^{(m)}[F\left(E_l - E_{fs}\right) - F\left(E_l - E_{fD}\right)] \qquad (2.28)$$

2.5 Mathematical Modeling for Capacitance-voltage (CV) Characteristics

The CV characteristics are determined from the device electrostatics. And the electrostatics of any system is described by the Poissons equation. The Poissons equation for MOS electrostatic potential is [68].

$$\varepsilon_0\varepsilon\frac{d^2v\left(y\right)}{dy^2} = q\left[p\left(y\right) - n\left(y\right) + \ N_D \ - N_A\right] \qquad (2.29)$$

Where n(y) and p(y) are the electron and hole concentrations, and N_D and N_A are the ionized donor and acceptor concentrations, respectively. is the relative dielectric constant and ϵ_0 is the free space permittivity. The electron concentration n(y) for n-MOS structure can be given by [68]

$$n\left(y\right) = \sum_{ij} N_{ij}|\psi_{ij}\left(y\right)|^2 \qquad (2.30)$$

and,

$$N_{ij} = \ \frac{n_{vi}m_{di}\ KT}{\pi\hbar^2}\ln\left[1 + \exp\left(\frac{E_F - E_{ij}}{KT}\right)\right] \qquad (2.31)$$

Here,N_{ij} is the carrier concentration in the jth subband of the ith valley, n_{vi} and m_{di} are the ith valley degeneracy and the density of state effective mass respectively. K is Boltzmann constant and T is the temperature. E_F is the Fermi energy, and E_{ij} and ψ_{ij} are the eigenvalue and eigen function of the jth energy level of the ith valley, which are obtained from the one dimensional solution of the Schrodinger equation. The Schrodinger of equation 2.1 along the confinement direction y, can be rewritten [68] for ith valley and jth subband as-

$$\left[-\frac{h^2}{2m^*}\frac{d^2}{dy^2} + V\left(y\right)\right]\psi_{ij}\left(y\right) = E_{ij}\psi_{ij}\left(y\right) \qquad (2.32)$$

At first equation 2.29 is solved using the semiclassical approximation assuming zero charge density, with Dirichlet boundary at the gate and Neuman boundary condition at the bulk, and then the charge density profile n(y) is determined combining equations 2.30, 2.31 and 2.32. In

our calculation 1st and 2nd eigen values are considered. The charge density profile is used to solve the Poissons equation and the process is repeated until self consistency is achieved.

Chapter 3

Simulation Results and Discussion

Chapter Outlines

- Current voltage (IV) characteristic of XOI FET

  - Channel Thickness dependent Performance

  - Impact of Interface Trap States

  - Channel material dependent performance (InGaSb vs InAsSb)

  - Effect of Different Gate Oxide having Same EOT

  - Traditional XOI FET vs Junctionless XOI FET

- Capacitance voltage (CV) Characteristic of XOI FET

  - Effect of channel thickness

  - Effect of channel composition

  - Effect of doping

  - Effect of temperature

3.1 Current voltage (IV) characteristic of XOI FET

The NEGF formalism required for the current-voltage characteristics starts from real space Hamiltonian H_0, that can be written in terms of effective mass [64]. But, when channel gets too thin, bulk effective mass remains no longer valid due to loss of translational symmetry along confinement direction. In that case nearest neighbor tight binding (TB) Hamiltonian, derived from $sp^3s^*d^5$ orbital basis, can be used. Figure 3.1 shows the dispersion relation of UTB GaSb obtained from TB model [69]. Since the growth along (001) direction is easiest, it has been considered to be the confinement direction, and [100] is taken as transport direction. Note here that the Γ valley offers lowest energy. Also, energy from four in (k_x-k_z) plane X valleys, projection of two X valleys with major axis along k_y (confinement direction), and projection of four L valleys are located well above in energy [70]. The same is also observed for InSb UTB [71]. Owing to large energy separations, only Γ valley contributes in transport through <001> oriented InGaSb UTB channel. Although bulk effective mass does not work, a modified effective mass can be used to construct the H_0, provided that it can reproduce the dispersion obtained from TB Hamiltonian. Using such modified effective mass for UTB offers great computational advantage over full tight binding simulation. Thickness dependent Γ valley effective mass of both GaSb and InSb are shown in FIG. 3.2 [69,71,72]. Analysis of the current-voltage characteristics are done using these thickness dependent effective masses, that are explained in next sections.

3.1.1 Channel Thickness dependent Performance

In our simulation, the wave function penetration is taken into account in the transverse direction (y axis in FIG. 2.1). It forces the wave functions to be zero, after penetrating into the oxide regions. With decreasing channel thickness, separation between eigen states increases. Therefore, for UTB devices, only the lowest eigen level (1st eigen) is present in the range of energy where the device operates. At zero gate bias (V_G), if the 1st eigen level is located several kT (thermal voltage) above the chemical potential at the source contact, the device provides lowest possible OFF-state current [73].

But, the actual position of the 1st eigen depends on the potential at the channel which is obtained from Poissons equation. At the vertical edge of the device (interface of gate and high-k oxide in FIG. 2.1), boundary to the Poissons equation is ($V_G + V_{bi}$), where V_{bi} is the built-in-potential. It is obtained from the work function of gate metal (Φ_m) and that of channel material (Φ_s) by [(Φ_m - Φ_s)/(-e)] in volt unit, where e is the electronic charge. Work function of alloyed metal can be tuned by tuning the alloy composition [74]. Making use of this fact, we first tune the position of 1st eigen level for each channel thickness at zero V_G so that same OFF-state current is obtained in each case. Then we calculate the thickness dependent I_D-V_G characteristics of the InGaSb XOI FET at a drain bias of 0.05 V, shown in FIG. 3.3. The body thicknesses used (along y direction of FIG. 2.1) is 3nm, 4nm, and 5nm. It is seen that use of bulk effective
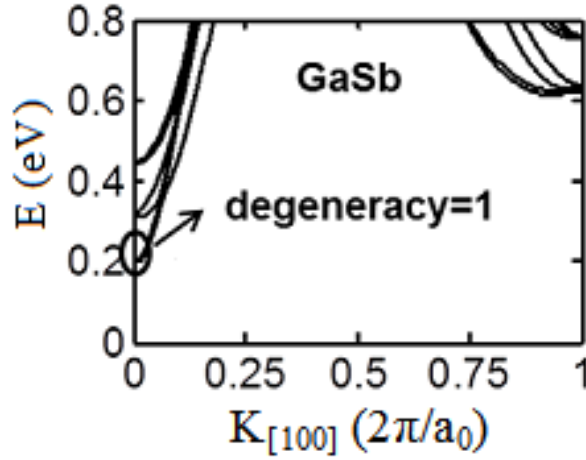
FIGURE 3.1: Tight binding dispersion of GaSb ultra-thin-body with (001) confinement and [100] transport direction. Figure is taken from [69].
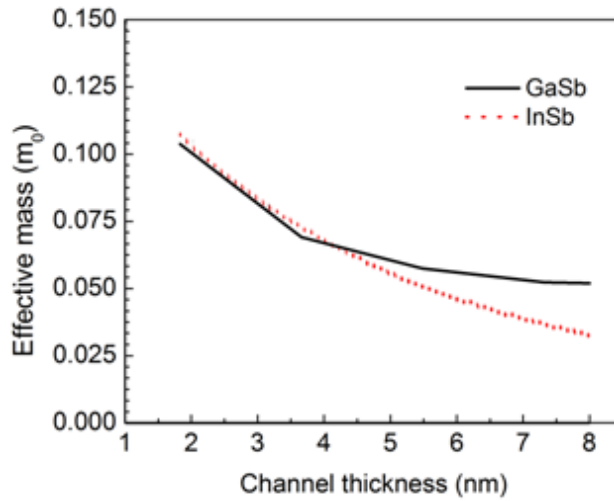
FIGURE 3.2: Thickness dependent effective mass at Γ valley of GaSb and InSb UTB with (001) confinement and [100] transport direction. Values taken from [69] and [71].

mass (m^*) significantly underestimates the drain current in each case. However, thinner channel gives higher current density (for either bulk or UTB m^*). This anomalous behavior can be well explained by the mechanism of carrier transport in ballistic regime [60,75]. Figure. 3.4 shows the 1st eigen value as well as the conduction band minima (E_C) for different channel thickness at V_G= 0.6 V. It is calculated along the transport direction x of our XOI FET (FIG. 2.1). Note that, the Fermi level (E_F) at the source contact (which represents its chemical potential) is kept fixed at 0 eV. Increasing the V_G from 0 V pushes the eigenvalues downward in energy. When the highest value of the 1st eigen goes below the source Fermi level (0 eV), the conduction of carrier takes place. It is attributed to the availability of energy states in between the chemical potential at source and drain contact and, evident from the energy dependent current spectrum shown in FIG. 3.4, as marked by J(E). Since the electrons had to overcome the enegy barrier for transport, the highest value of the 1st eigen dominates the conduction process.

The highest value of E_C as well as that of 1st eigen of the device, along its thickness (y direction
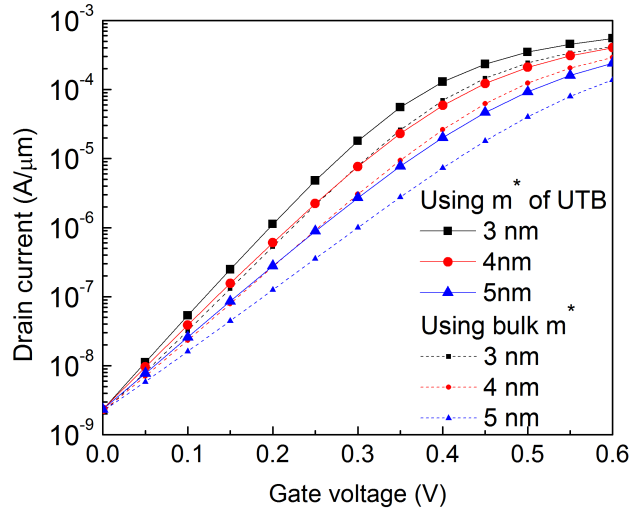
FIGURE 3.3: I_D-V_G characteristics of 15nm InGaSb XOI nFETs for different channel thickness at a drain bias of 0.05 V.The structure of the devices is shown in FIG-2.1.
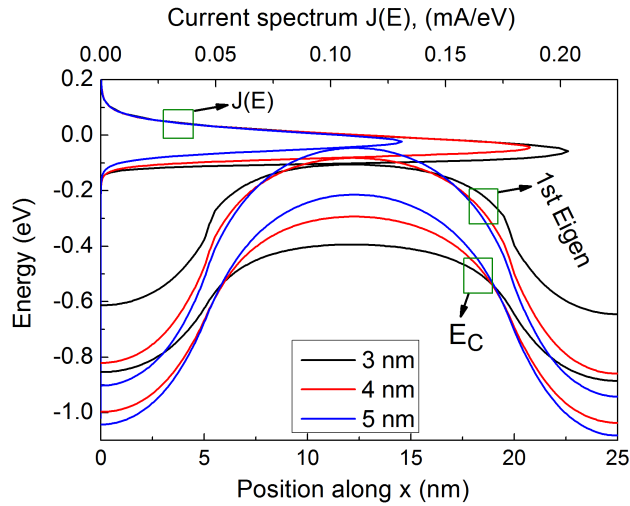
FIGURE 3.4: For InGaSb XOI nFET at V_G=0.6V, the conduction band diagram (E_C) and the 1st eigen level along the transport direction of the channel. Energy dependent current spectrum J(E) is obtained at the center of the channel.

in FIG. 2.1) is shown in FIG. 3.5. It is calculated at $V_G = 0.6$ V. In contrast to 4 and 5 nm channels, the 3 nm channel possesses a flat-band profile. This is attributed to the uniform potential distribution along the thickness of 3 nm channel [49]. Owing to the uniformity, the potential droped across the 3 nm channel is totally utilized to move its eigen value downward. But in relatively thicker channel (4 and 5 nm), a portion of the potential drop causes the band to bend, and the remaining is utilized to move the eigen value downward. As a consquence, the 1st eigen level of the thinnest channel (3 nm) is located at the lowest energy with respect to the Fermi level (0 eV). Consequently, more energy states of the 1st subband are available, thereby relatively larger amount of carrier can participate in the conduction process in the thinner channel. On the other hand, speed of these carrier in conduction (known as injection velocity) is determined by the dispersion relation at the channel [76].
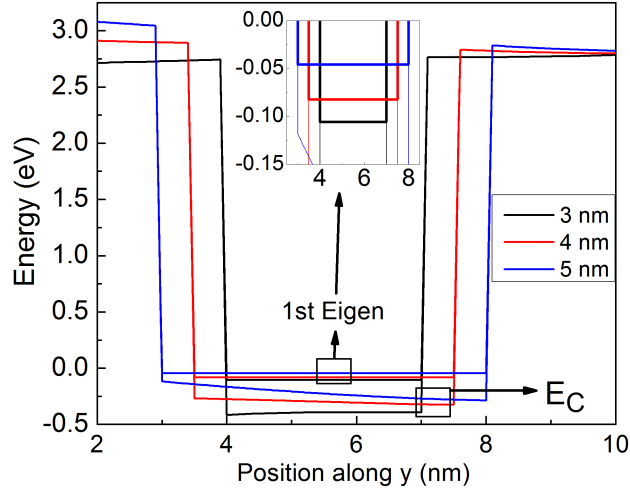
FIGURE 3.5: Conduction band diagram and the 1st eigen energy across the transport direction of the channel. They are calculated at the center of the channel at $V_G = 0.6$ V. Inset shows the 1st eigen energy of the device.

Because of the non-parabolicity in the dispersion, the effective mass in UTB channel becomes slightly higher than bulk one [77]. Since the havier particle moves relatively slowly, use of thickness dependent effective mass leads to relatively small injection velocity. Nevertheless, when the confinement direction of the UTB is taken along the semi-major axis of energy ellipsoid (for L or X valley), injection velocity of thinner channel becomes higher. It is because, the heavy confinement mass brings the lowest eigen value of those valleys to the minimum, therefore, they are more likely to be occupied by traveling electrons. And the light transport mass of those occupied valleys ensures the high injection velocity. However, if the UTB is not thin enough, valleys with lighter confinement and heavier transport mass could be occupied, leading to overall smaller injection velocity [76]. Note that, the Γ valley does not impose such paradigm because of its isotropic dispersion relation. Overall, the combined effect of Γ and L valley ensures the increase in injection velocity with decreasing channel thickness, although in general it depends on the orientation of UTB channel.

3.1.2 Impact of Interface Trap States

III-V materials do not have their native oxide as Si has its SiO_2. Therefore they possess a large number of interface trap states at the channel-gate oxide and channel-BOX interface. Occupation of these states, i.e., concentration of trapped charge and their polarity depends on the charge nutrality level (CNL) and Fermi level, E_F [78,79]. Traps are acceptorlike (-/0) in upper gap (from middle of the band gap to CBM) and donorlike (0/+) in the lower gap (from middle of the band gap to VBM) [79]. Therefore if CNL lies bellow the CBM of a nFET, in respond to increasing positive gate bias, E_F goes above CNL. Consequently negative charge accumulates at the interface states. For example, the CNL of both GaSb and InSb, and therefore that for InGaSb lies well below the CBM [80], leading to the formation of negatively charged interface states. Linearly interpolating the result from tight binding study [80], the
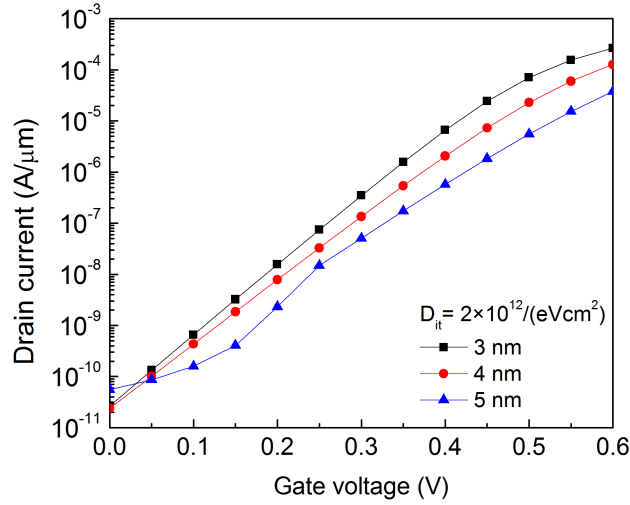
FIGURE 3.6: I_D-V_G characteristics of 15 nm InGaSb XOI nFETs at presence of interface trap states density, $D_{it}= 2\times10^{12}$eV^{-1}cm^{-2}.

CNL of $In_{0.3}Ga_{0.7}$Sb is found to locate 0.398 eV below the CBM. Density of trap states (D_{it}) is minimum at CNL and generally increases toward CBM as a parabolic function of energy. However, D_{it} concentration greatly depends upon the processing and passivation technique. Ohtakeet et al. recently reported a novel processing technique that can obtain the D_{it} of HfO_2/GaSb interface to be 2×10^{12}eV^{-1}cm^{-2} [81]. Also, Passivation using $(NH_4)_2$S [82] offers almost uniform distribution of D_{it} in the range of energy from CNL to CBM. In our simulation we assume same D_{it} concentration on channel-gate oxide and channel-BOX interface. BOX-substrate interface is not considered because Si/SiO_2 interface is so perfect that offers negligibly small D_{it} concentration. Figure 3.6 shows the I_D-V_G characteristic of our device at $D_{it} = 2\times10^{12}$ eV^{-1}cm^{-2}. It is seen again at presence of D_{it}, thinner channel performs better.

However, comparing this I_D-V_G characteristic with FIG. 3.3, it is shown in FIG. 3.7 (a) that, ON-state current for each channel thickness is reduced significantly (more than half) owing to the presence of D_{it}. Figure 3.7(b) and 3.7(c) shows the variation of threshold voltage (V_T) and subthreshold slope (SS) respectively as a function of channel thickness. In the absence of interface states, the V_T (value of V_G for which I_D is 30 nA) decreases from 0.1035 V to 0.072 V, and the SS decreases from 95.65 mV/dec to 72.84 mV/dec for decreasing the channel thickness from 5 nm to 3 nm. Without perturbing this trend, interface traped charge increases the V_T and slightly decreases the SS. Figure 3.7 (d) shows the DIBL of the XOI FET under study. For zero D_{it}, it is found to decrease from 0.1764 mV/mV to 0.0768 mV/mV for decreasing the channel thickness from 5 nm to 3 nm.

Although interface charge deteriorates device performance, exploring the interaction of this charge will lead to possible solution. Interface trapped charge are simply added to the right side of Poissons equation and affects the channel potential. Negative trapped charge reduces the potential and pushes the eigen values upward from where they were in absence of D_{it} (FIG. 3.5).
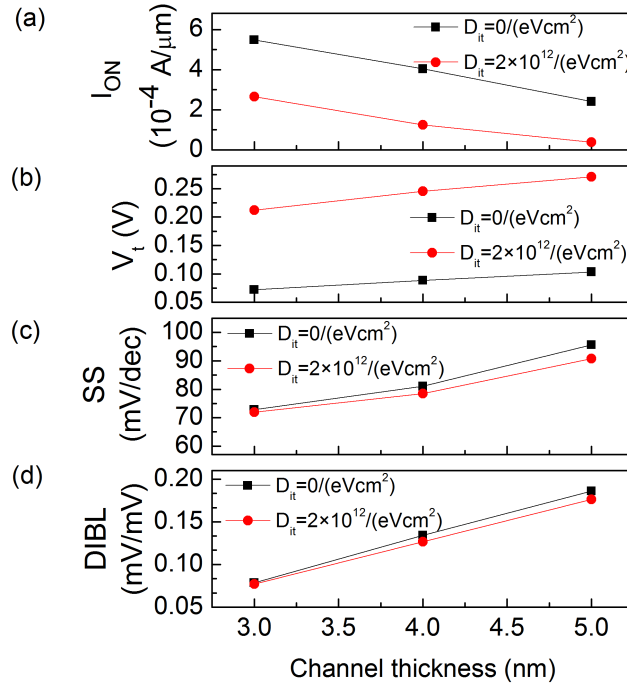
FIGURE 3.7: Ballistic performance comparison of InGaSb XOI nFET having 15 nm gate length, a) On state current, b) Threshold voltage, c) subthreshold slope, d) DIBL of the device.
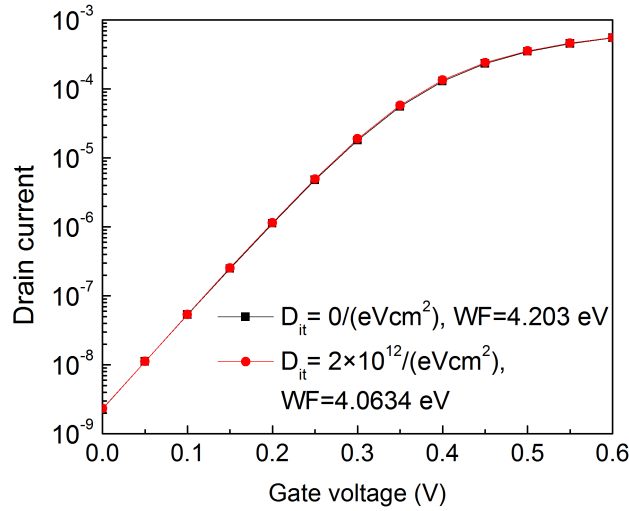
FIGURE 3.8: I_D-V_G characteristics of 3 nm thick InGaSb XOI nFETs with different gate metal work function (WF) and interface state concentration.

As a consequence drain current gets reduced. If we somehow can move the eigen value to its old position, we will again get our desired drain current. Reduction of gate metal work function Φ_m does so by adjusting the V_{bi}. For 3 nm channel thickness, when Φ_m is reduced from 4.203 eV for perfect interface to 4.0634 eV for $D_{it} = 2 \times 10^{12}$ eV^{-1}cm^{-2}, the device offers exactly same performance as shown in FIG. 3.8. It further means the impact of D_{it} can be compensated. Because of the position of CNL (that lies bellow CMB) of the InGaSb, nFETs made of this material are very sensitive to interface states, and has been assumed to be good for pFET only. And a combination of InGaSb pFET and InAsSb nFET is necessary to implement a XOI based CMOS [83] for ultra-low-power logic application. However at ballistic limit, InGaSb based

nFETs offer better logic figure of merits [84]. Also our study shows their sensitivity to interface states can be compensated. Therefore it is possible to materialize CMOS solely with a InGaSb XOI based system.

3.1.3 Channel material dependent performance (InGaSb vs InAsSb)

Any field effect transistor having a gate length less than 100 nm can behave in a very different way. For example InAsSb long channel MOS shows better performance than that of InGaSb due to higher electron mobility [4,45]. However, when the channel length goes to sub 20 nm regime the electronic transport through the channel is purely ballistic. In that case, concept of mobility does not apply but the drain current is determined by different dominating factors [60,85]. In that case, InGaSb completely outperforms the InAsSb as shown in FIG. 3.9. In this figure, the comparison of I_D-V_G characteristics of InGaSb and InAsSb XOI FETs plotted at V_D=0.05V. The body thickness of the device is 3nm. Wave function penetration in the oxide region is also taken into account. To compare the performance, first the OFF current of the devices are made equal by tuning the gate metal work function, Φ_m. It is clear from the figure that, the drain current, for InGaSb is higher than that obtained for InAsSb at each gate bias. It is because, when device size shrinks down to the ballistic limit, carrier goes through the channel facing negligibly small or no scattering. Since current is defined as the amount of charge transferred per unit time, the ballistic current is simply determined by two factors, i) how much charge is there in the channel moving, ii) the transit time of the carrier through the channel [85]. The second factor also means the current is proportional to the carrier velocity. But the traveling carriers can have different allowed velocities through the channel, and to find the total current, summation of the currents given by each allowed velocities are to be taken. In another sense, integral over the entire energy range of traveling carriers must be taken when current components are expressed in terms of energy. Amount of carrier in the channel depends on the density of states (DOS). For InGaSb and InAsSb materials the effective density of states are evaluated using linear interpolation from the values experimentally measured for the binaries [86], and found to be 1.93×10^{17} and 1.05×10^{17}, respectively.

Again, any heavier particle tends to move slowly, i,e the velocity of electron is inversely proportional to the effective mass (m^*). More accurately speaking, it is proportional to the inverse of square root of m^* for a given energy of traveling electron. Therefore combining the two influential factors, it can be argued that the ratio of effective DOS to m^* would determine the amount of current through the device. This ratio for InGaSb is found to be 1.225 times higher than that of InAsSb. That is why InGaSb XOI FET gives higher current than InAsSb XOI FET. Not only higher drain current, the I_D-V_G characteristic in FIG. 3.9 also shows the drain current for InGaSb increases more sharply than InAsSb. This behaviour could be easily understood from semiclassical Top of the barrier or TOB model of ballistic transport. The highest point of electronic potential (band diagram) in the channel is called the Top of the barrier, which is
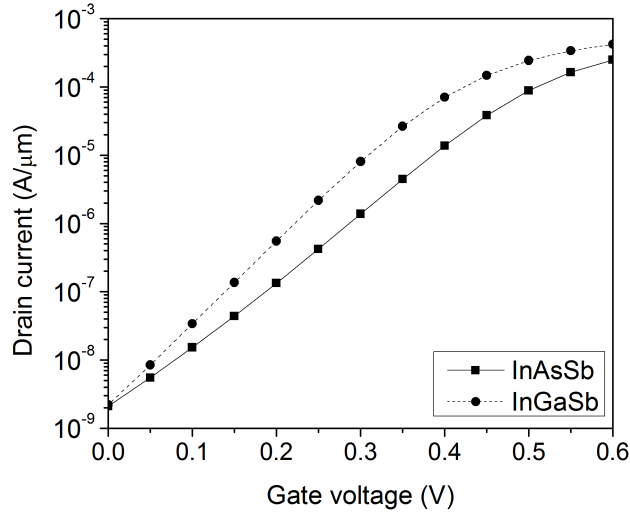
FIGURE 3.9: I_D-V_G characteristics of 15nm InGaSb and InAsSb XOI nFETs. The structure of the devices is shown in fig. 2.1.

evaluated from self consistent electrostatics. According to this model, the drain current is given by [87]

$$I_D = \frac{W2q}{h} \int_{E_C}^{\infty} \sqrt{\frac{2m^*E}{\pi\hbar}} [f(E) - f(E - V_d)]dE \tag{3.1}$$

Here, W is the width of the device, f(E) is the fermi function with respect to the chemical potential at the source, f(E-qV_d) is the fermi function with respect to drain chemical potential. E_C is the position of TOB, and the above integral gives the on state current. Integral of the same equation, using the limit from negative infinity to TOB determines the subthreshold current, which is mainly leackage or tunneling of carrier from source to drain [88]. That is why position of TOB actually determines the subthreshold as well as off state current. This position of TOB is tuned by tuning gate metal work function Φ_m to get same I_{OFF} for both materials. Equation (3.1) shows that the drain current is proportional to the square root of the effective mass. Further, the rate of change of current with respect to gate bias also has similar proportionality relation. Since InGaSb possess slightly higher effective mass, current increases much sharply leading to lower subthreshold slope (SS), and finally saturates at a higher value in case of InGaSb XOI FET.

Figure. 3.10 shows the SS which is reduced from 97.186 to 82.351 for changing the material from InAsSb to InGaSb. Figure. 3.11 shows the variation of threshold voltage of InGaSb and InAsSb XOI nFETs as a function of the ratio of effective density of states to effective mass. It is found that InGaSb gives lower threshold voltage than InAsSb. The threshold voltage as well as the OFF current of the device depends on the barrier height at zero gate bias. This barrier height can be controlled by the work function of the gate metal. It is important that, we tuned
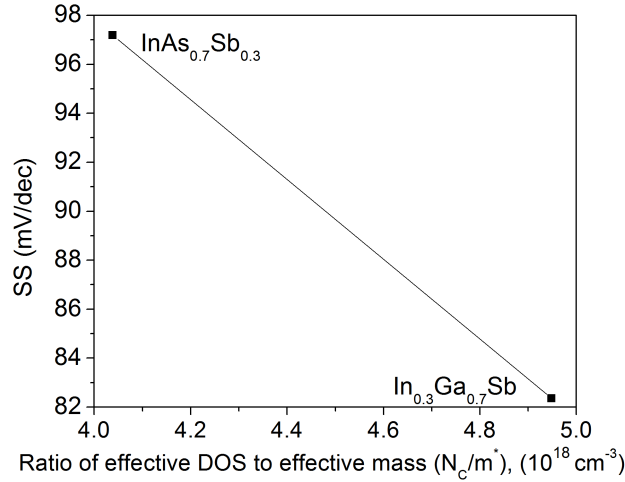
FIGURE 3.10: Variation of Subthreshold slope (SS) with the ratio of effective DOS (density of states) to m* (effective mass).
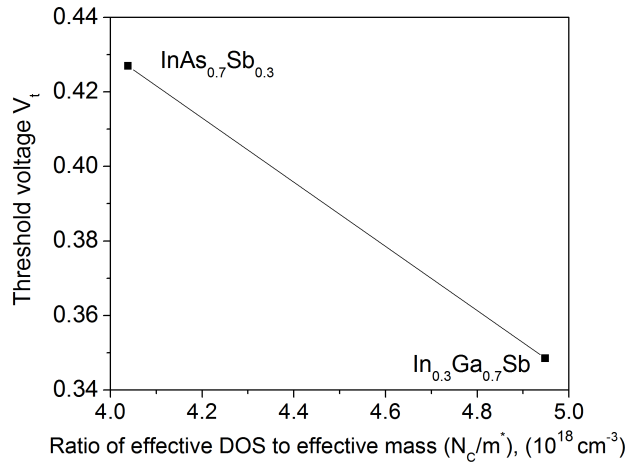
FIGURE 3.11: Variation of threshold voltage with the ratio of effective density of states to effective mass. The workfunction the gate metal is tuned to give the same OFF current for InGaSb and InAsSb materials.

the work function of the gate contact to make the OFF current equal for both cases so that other parameters can be compared.

3.1.4 Effect of Different Gate Oxide having Same EOT

Different high-k dielectrics are supposed to provide same device performance if their physical thickness are not equal but equivalent, called Equivalent Oxide Thickness (EOT). For ultra thin body (UTB) devices like XOI, there is no quasi-neutral region in the channel which makes the channel fully depleted. That is why the flat band potential depends both on the surface potential at both channel-gate oxide and channel-buried oxide interfaces. However, band offset plays an important role in determining the IV characteristic, even when different gate oxides of same EOT are used. To illustrate this scenario, the I_D-V_G characteristics plotted at V_D=0.05 V of the InGaSb XOI FET using two gate dielectrics are shown in FIG. 3.12. The two dielectrics
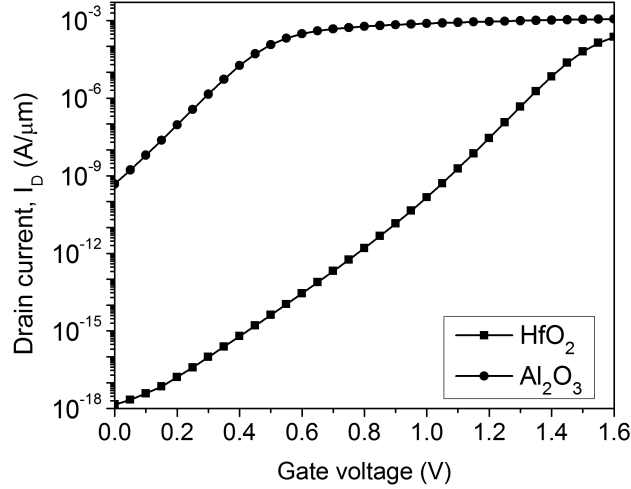
FIGURE 3.12: I_D-V_G characteristics of 15nm InGaSb XOI nFETs using HfO_2 and Al_2O_3 gate oxides. The structure of the devices is shown in FIG. 2.1.

used here is HfO_2 and Al_2O_3. The body thickness of the device is kept 3 nm. Wave function penetration in the oxide region is also taken into account. It is found that for HfO_2, the drain current is lower than that of Al_2O_3, although they have same EOT of 0.5 nm. Generally if two gate oxides have the same EOT, the same oxide capacitance, and thereby same electrostatic control over the channel and hence identical device performance is expected. But in case of XOI structure, the deviation is found because of conduction band discontinuity (ΔE_C) between the oxide and the channel.

It has been stated previously that the ballistic current depends on the position of TOB, while the source Fermi level is kept fixed (which is at 0 eV in our study). When the gate metal work function is kept fixed (which is greater than 4 eV in our study), lower (ΔE_C) implies the higher difference between Fermi level at the source contact and the TOB in the channel. This further implies lowest number of energy states are available for conduction at every gate bias. Since lower number of states available for conduction leads to lower drain current, lower conduction band offset between oxide and channel results to lower drain current, provided that Φ_m is kept fixed. For $In_{0.3}Ga_{0.7}$Sb channel, $\Delta E_C(Al_2O_3) = 2.88$eV and $\Delta E_C(HfO_2) = 1.76$eV [80]. That is why HfO_2 is giving lower drain current despite of same EOT. Since the TOB is situated at different levels under zero gate bias, we carried out the simulation for a wide range of gate bias to ensure the turn ON of both devices. But in real life application both devices could be operated at a much less bias range by tuning the gate work function. The I-V curve shown in FIG. 3.12 for HfO_2 can be shifted to the left by reducing Φ_m used for HfO_2 based device. And, if it were choosen to be 1.12eV less than that used for Al_2O_3 based device (since $\Delta E_C(Al_2O_3)$-$\Delta E_C(HfO_2)$=1.12 eV), the two curves will be at their closest position. To understand the effect of ΔE_C only, other influential factors like Φ_m are so choosen that causes the energy band inside the oxide to start from the same maximum height. Figure 3.13 shows the change in subthreshold slope (SS) as a function of ΔE_C between oxide and the channel. It is found that the subthreshold slope decreases with decreasing ΔE_C.
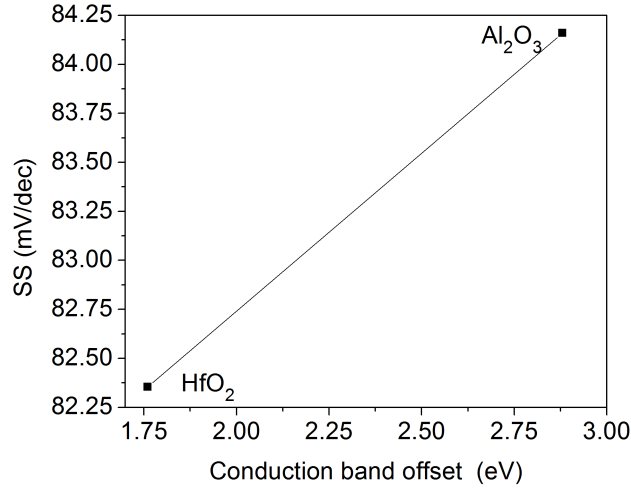
FIGURE 3.13: Variation of subthreshold slope (SS) of InGaSb XOI FET for HfO_2 and Al_2O_3 gate oxides.
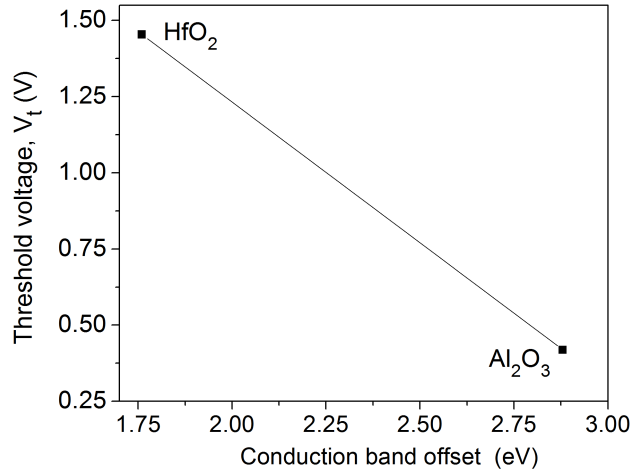
FIGURE 3.14: Variation of threshold of InGaSb XOI FET for the use of HfO_2 and Al_2O_3 as gate oxides.

The lower SS implies the sharp change of drain current with gate bias and the better electrostatic control of gate over the channel. Better control of gate also indicates the lower influence of drain voltage on I-V characteristic and hence supressed short channel effect (SCE), like drain induced barrier lowering. FIG. 3.14 shows the variation of threshold voltage as a function of ΔE_C between oxide and the channel. It shows the threshold voltage decreases with increasing ΔE_C. For HfO_2 gate oxide, the threshold voltage found in our case is 1.454V, which is not acceptable. But it can be brought very close to zero by gate work function engineering, so it is not a problem at all. The present study reveals that there is a great impact of ΔE_C on the SS and the threshold voltage.

3.1.5 Traditional XOI FET vs Junctionless XOI FET

Traditional devices like bulk MOSFET to SOI (or even the experimentally demonstrated XOI till to date) have been using junctions to control the carrier flow through the channel. The pn
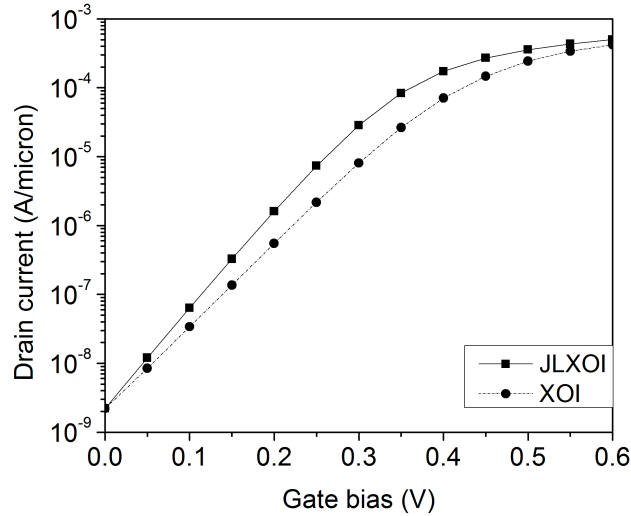
FIGURE 3.15: Comparison of I_D-V_G characteristics of 15nm InGaSb XOI and JLXOI nFET. Structure of the device is shown in FIG. 2.1.

junction is most common, which is formed by n type contacts and a p-type channel region or vice versa. This junction forms a barrier along the channel, height of which is controlled by gate bias. Thereby modulation of the amount of carrier flow is being done [89]. But when device size shrinks to 22 nm regime or even further, formation of junctions becomes very challenging. Extremely sharp doping concentration gradients are required in junctions. Typically the n type concentration must switch from $1{\times}10^{19}$/cc to p-type concentration of $1{\times}10^{18}$/cc, within a couple of nanometers. This imposes severe limitations on the processing thermal budget and necessitates the development of costly millisecond annealing techniques [89, 90]. The possible solution is making a device with no junction, in which the doping concentration in the channel is exactly same as that in source and drain region. When the channel with such doping profile is thin and narrow enough to allow the full depletion of carriers, performance of the device can be made comparable with traditional devices having junctions [89]. Availing the advantage of junction less architecture, performance of double gate and multi gate transistor has been studied recently [90,91,92,93]. But all of these devices have 3D structure and therefore fabrication process is complicated, where XOI has the simple planner architecture in contrast.

I_D-V_G characteristics for InGaSb XOI and JLXOI are compared in FIG. 3.15. The results are obtained for V_D=0.05V. Gate work function engineering also applied here to tune the OFF state current. Thickness of the channel is taken to be 3nm. Wave function penetration in the oxide region is also taken into account. The figure shows that the drain current for JLXOI is higher than that of XOI structure for all positive gate bias. It is attributed to the way of carrier transport through the channel. In case of XOI, carriers are unable to transport from the source to the drain at OFF state due to the barrier of pn junction, which is formed at the interface of heavily doped (n type) source and lightly (p type) doped channel. The height of this barrier is controlled by the gate bias. With increasing gate bias, barrier height decreases allowing current to flow through the channel [87]. In case of JLXOI, junction induced barrier is
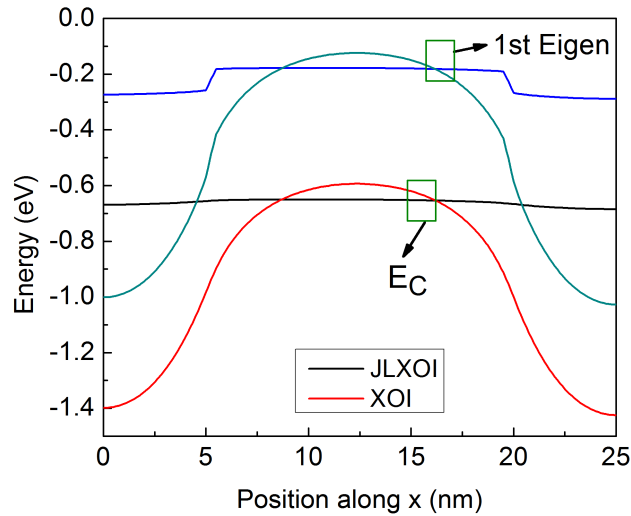
FIGURE 3.16: Conduction Band diagram and 1st eigen level along the channel for XOI and JLXOI nFET.
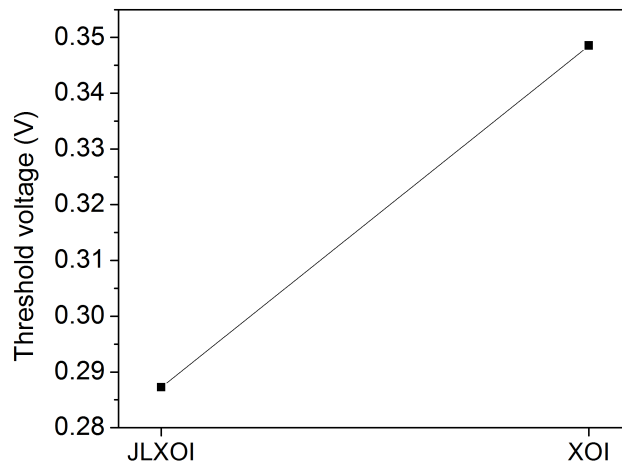
FIGURE 3.17: The threshold voltage for 15 nm InGaSb XOI and InGaSb JLXOI nFET. FIG. 2.1 shows the actual device structure

not formed. Rather the band diagram along the channel is essentially flat due to the uniform doping profile. This flatness may be disturbed by the boundary imposed by gate metal work function, but still in comparison with XOI, it remains almost flat as shown in FIG. 3.16. When the band is significantly above from the Fermi level at the source, no electron will be injected in the channel, leading to zero current, or the OFF state of the device. But when it is below the source fermi level, carriers can be injected and move through the channel. However, the barrier of XOI device is narrow in comparison with the JLXOI (FIG. 3.16). That is why to have same OFF state current, height of the barrier for XOI FET needs to be bigger to supress the carrier tunneling, which is mainly responsible for determining the OFF state as well as subthreshold current [88]. For the same reason the TOB for JLXOI lies below than that of XOI, and it is closer to the fermi level at the source contact (which is kept fixed at 0 eV).

The gate bias causes both TOB and 1st eigen to move down in energy. At the ON state, both the TOB and 1st eigen of JLXOI goes more below than that of XOI. That is why, JLXOI
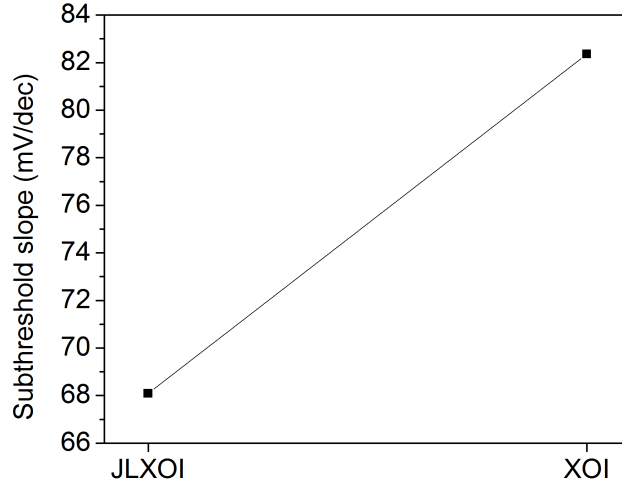
FIGURE 3.18: Subthreshold slope of 15 nm InGaSb XOI and Junction less XOI (JLXOI) nFET. Device structure is shown in FIG. 2.1.

offers more current at the ON state, while OFF current has been made equal. Nature of the conduction band is also responsible for determining the threshold voltage of two devices. Since TOB of JLXOI lies bellow with respect to XOI, the JLXOI turns on at a lower voltage, offering lower threshold for JLXOI. The threshold voltage for both devices is compared in FIG. 3.17. The I_D-V_G characteristics presented in FIG. 3.15 also shows that the drain current of JLXOI FET increases more sharply than that of XOI. It means the subthreshold performance is better for JLXOI. Lower value of SS means better performance and the lowest value of SS is 60 mV/dec at room temperature. Although 60 mV/dec SS means the best possible control of gate over the channel, the value less than 90 mV/dec is acceptable for logic application. The SS for both XOI and JLXOI devices is shown in FIG. 3.18 in which the XOI gives 82.351 mV/dec SS where as JLXOI gives SS of 68.088 mV/dec. It reveals that the JLXOI offers near ideal performance, even at 15 nm gate length. The lowest SS reported to date is 63 mV/dec, but is is obtained for tri gate SOI transistor [25]. Tri gate devices need 3D structure which is difficult to fabricate. In contrast the JLXOI is a planer device offering near ideal performance with well established and simple fabrication process.

3.2 Capacitance voltage (CV) Characteristic of XOI FET

One of the main challenges of XOI FET is to optimize the interfacial (i.e., gate oxide-channel, channel-buried oxide and buried oxide-substrate) charge properties. Channel thickness of an ultra-scaled XOI device needs to be few nanometers for the better control and high I_{ON}/I_{OFF} ratio. However, too much reduction in channel thickness would cause the interface charge properties to dominate the device performance [43, 94]. The electron-phonon scattering and phonon limited mobility degradation becomes prominent for very thin channel devices [47], which is recently demonstrated for the InAs based XOI FET also [73]. Moreover, interface
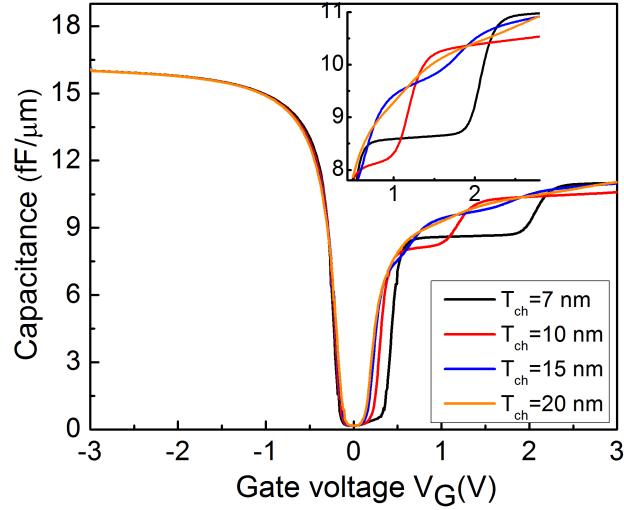
FIGURE 3.19: CV profile of $In_{0.3}Ga_{0.7}$Sb XOI FET as a function of channel thickness.

traps close to or beyond the conduction band edge can alter the carrier density and transport properties [45]. That is why quality of interface of any XOI device must be carefully studied after the fabrication. The quality of the interface and therefore the transport properties of the channel can be well understood from its capacitance-voltage (CV) characteristics. Although the CV characteristics of SOI FET have been well understood, it has not comprehensively studied for XOI FETs. Here, a comprehensive study on the CV characteristics of InGaSb XOI FET is presented in order to demonstrate and optimize the interface properties.

3.2.1 Effect of channel thickness

Channel thickness-dependant CV characteristics with respect to the gate bias are shown in FIG. 3.19. Here note for the 7nm thickness (or in FIG. 3.21), the gate capacitance increases from its minimum value for VG from 0.0 V to 0.7 V and then remains constant up to $V_G = 2.1$ V. This constant capacitance is denoted as 1st step constant capacitance region (CCR). After 1st step CCR the gate capacitance further increases and then remains constant up to the gate bias of 3.0 V. This region is defined as 2nd step CCR. This staircase behavior in the CV characteristics of the XOI FET is quite different from that reported for conventional SOI and bulk MOSFETs [95, 96]. With increasing thickness, the CV curves shift towards left. Also note for the thicknesses of 15 nm and above, the CCRs are vanished and CV curves show same trend as SOI and bulk MOSFET [96].

In order to explain the anomalous nature in CV curves, channel thickness-dependent conduction band profiles as well as 1st and 2nd eigen energy levels are plotted in FIG. 3.20 (a) for V_G=3 V. Here note that the finite quantum well structure of XOI FET causes the energy eigen level to be descrete and it brings subbands at the channel. Occupation of these subbands depends on the relative position of Fermi level E_F and eigen level E_{ij}. With increasing gate bias (V_G), the eigen levels move downward (since Fermi level is kept fixed at 0 eV). When an eigen level
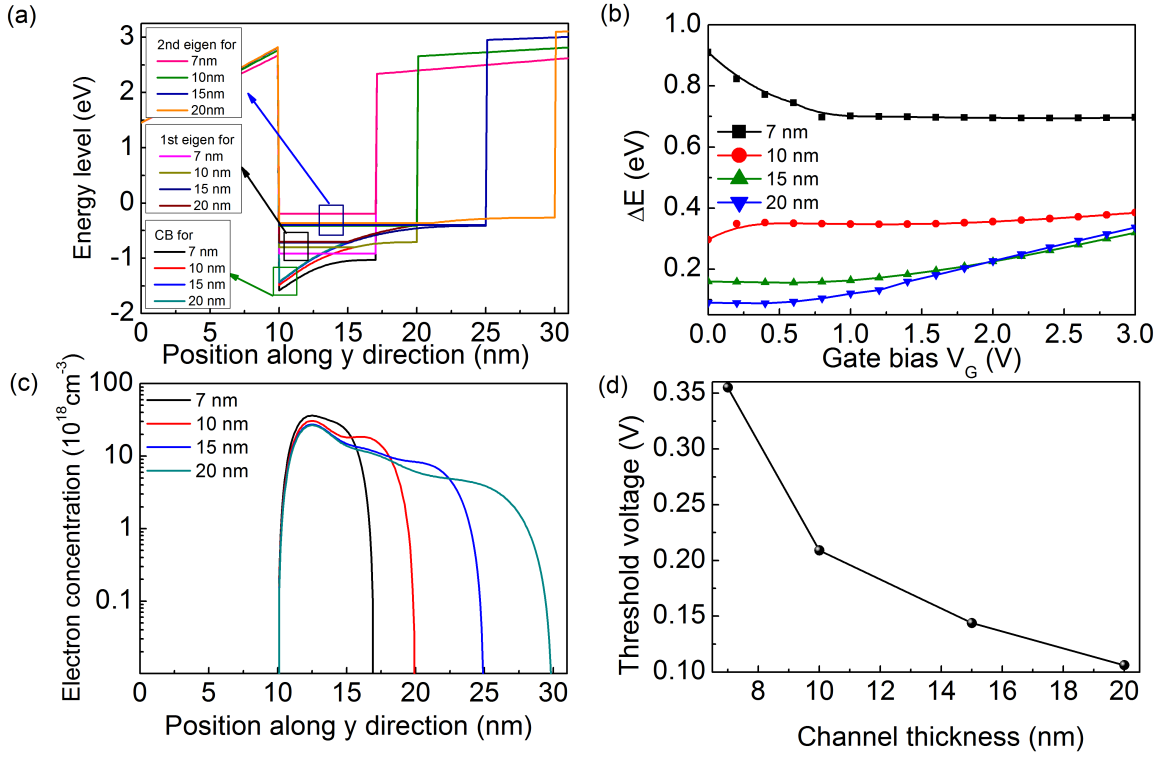
FIGURE 3.20: Channel thickness dependent performance of InGaSb XOI FET, (a) Band diagram along with 1st and 2nd eigen levels, (b) Difference between 1st and 2nd eigen at different gate bias, (c) Electron distribution inside the channel at V_G=3 V, (d) Threshold voltage as a function of channel thickness. The positions in the figures are measured from the gate-oxide interface along y direction as shown in FIG. 2.1

goes below the Fermi level, it gets populated. At lower channel thickness (less than 10 nm), the difference between eigen states is quite high, which is shown in FIG. 3.20 (b) for different V_G. Therefore, when the Fermi level crosses the 1st eigen state and lie in between 1st and 2nd, only 1st eigen level contributes to the total charge in the channel. Owing to low density of states of III-V material and a single subband contribution, bias dependent charge increment is small enough to make the capacitance constant, leading to 1st step CCR. With further increase in gate bias, the Fermi level goes over the 2nd eigen state, hence both 1st and 2nd subbands contribute and cause a jump in the total charge in the channel. Therefore, the capacitance changes from 1st step to 2nd step CCR (FIG. 3.19). But, if the eigen energy states are close to each other, carriers can move smoothly in subbands. For channel thickness 15 nm or above, the difference between eigen levels gets lower enough for the smooth intersubband transition of carrier. As a result no steps or CCRs are observed in the CV characteristics at high channel thickness (FIG. 3.19).

FIG. 3.20 (b) also shows that the difference between eigens is not constant but changes with V_G owing to the bending of conduction band with it. Also it gets lower with increasing channel thickness for V_G<2 V. For V_G>2 V, the 15 nm and 20 nm channel shows opposite trend. It is because at high gate bias, more carrier accumulates in the 1st subband and their electrostatic repulsion pushes the closely located 2nd eigen a little bit away. Figure 3.20 (c) shows the electron

FIGURE 3.21: Channel composition dependant CV characteristic of $In_xGa_{1-x}Sb$ XOI FET.
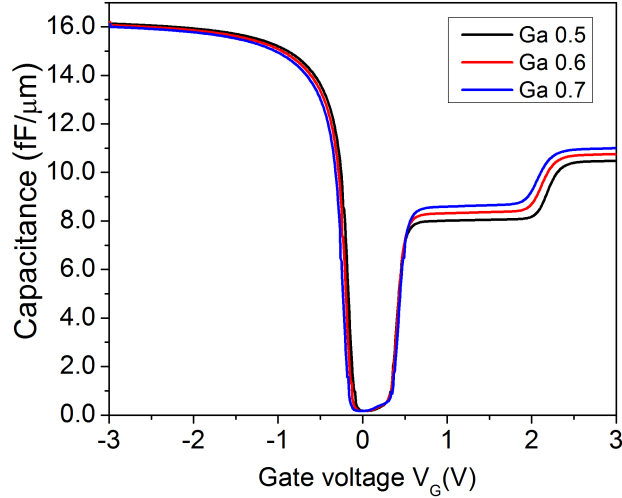
concentration in the channel for V_G=3 V where peak electron concentration is observed at the high-K oxide-channel interface and then gradually reduced along the channel thickness. With increasing thickness, the rate of reduction also found to be increased. In fig. 3.20 (d), channel thickness dependent threshold voltage (V_T) is presented, that has been determined from the tangent of CV curves that intercept the positive voltage axis. The V_T decreases with increasing channel thickness, attributed to the lowering of 1st eigen with it which is evident from fig. 3.20 (a).

3.2.2   Effect of channel composition

Figure. 3.21 shows the channel composition dependent CV characteristics as a function of gate bias (V_G). The capacitance remains almost composition independent up to $V_G = 0.5$ V. After that, it increases in each CCR with increasing gallium (Ga) composition. This increment is owing to the increase in density of states with increasing Ga composition. For enhancement mode devices which are mostly used, performance at negative gate bias is not the point of interest.

Figure 3.22 (a) shows the composition-dependent conduction band profiles as well as 1st and 2nd eigen energy for VG=3 V. The large separation between 1st and 2nd eigen causes the CCRs to appear in the CV curves.

To elucidate the 1st and 2nd step CCR (FIG. 3.3) more, the composition dependent 1st and 2nd eigen energies are plotted in FIG. 3.22 (b) with respect to electric field that exists at the gate-oxide and channel interface. It reveals that the difference between 1st and 2nd eigen energies for a given surface electric field (or respective gate bias) decreases with increasing Ga composition. Consequently, the required gate bias for the transition from 1st to 2nd step CCR decreases with increasing Ga composition, causing the CV curves to shift toward left (FIG. 3.21). Figure 3.22 (c) and (d) show the electron distribution and the peak electron concentration, respectively, for
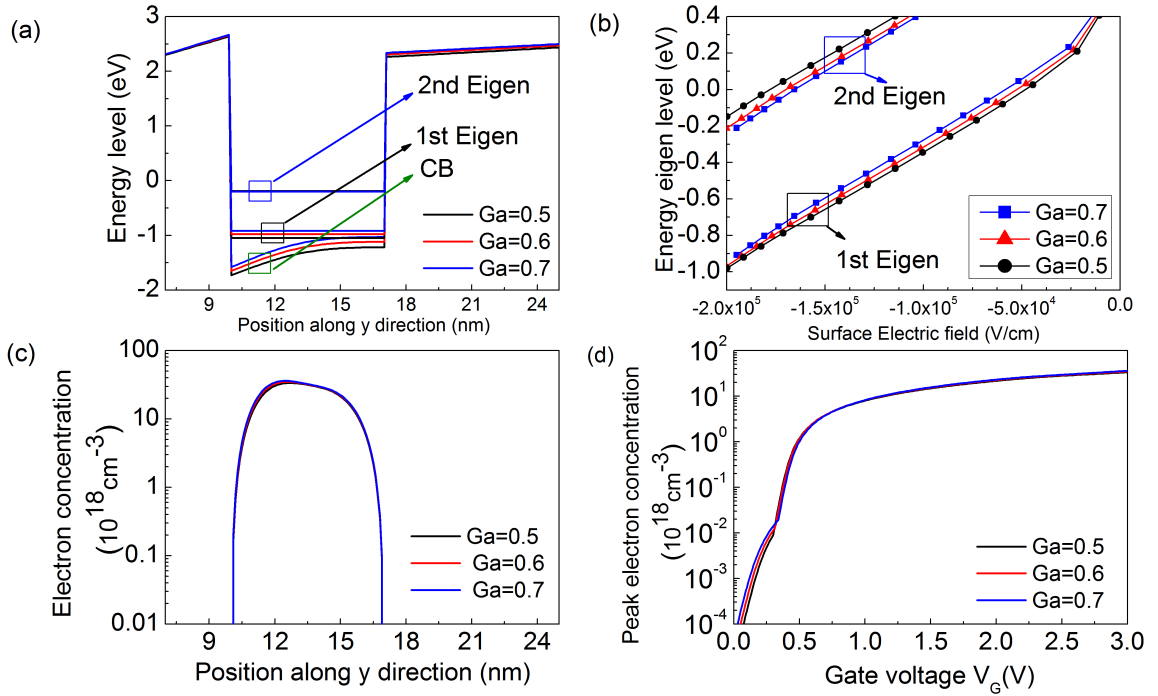
FIGURE 3.22: For different channel compositon of In_xGa_{1-x}Sb XOI FET, (a) Band diagram as well as 1st and 2nd eigen energy states of the device for V_G=3 V, (b) 1st and 2nd eigen energy states as a function of electric field at gate oxide-channel interface, (c) Electron distribution inside the channel at V_G=3V, and (d) Peak electron concentration of the channel for different gate bias. The positions in the figures are measured from the gate-oxide interface along y direction as shown in FIG. 2.1
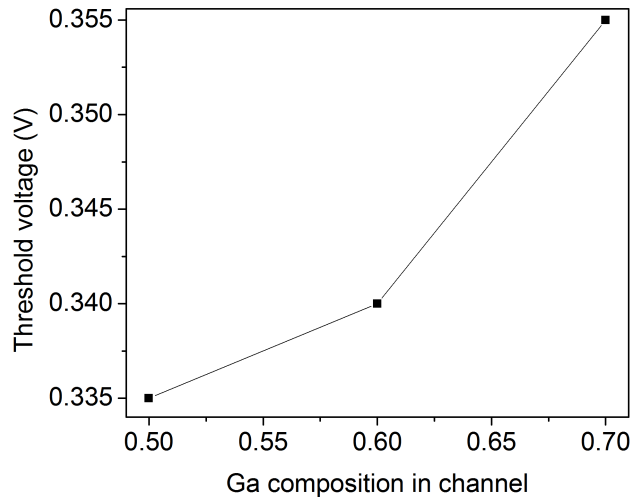
FIGURE 3.23: Threshold voltage as a function of Ga composition.

different Ga compositions in the channel. The dome shaped distribution of electrons inside the channel observed here is in agreement with reported studies on InAs for channel thickness below 10 nm [97]. Note that the peak electron concentration increases with increasing Ga composition. Also note that there is a sudden sharp increase in peak electron concentration for gate bias from 0.3 V to 0.7 V, and then it changes slowly, and finally, saturates at higher gate bias (3.0 V) as shown in FIG. 3.22 (d). It is because of the step wise occupation of eigen levels explained previously.
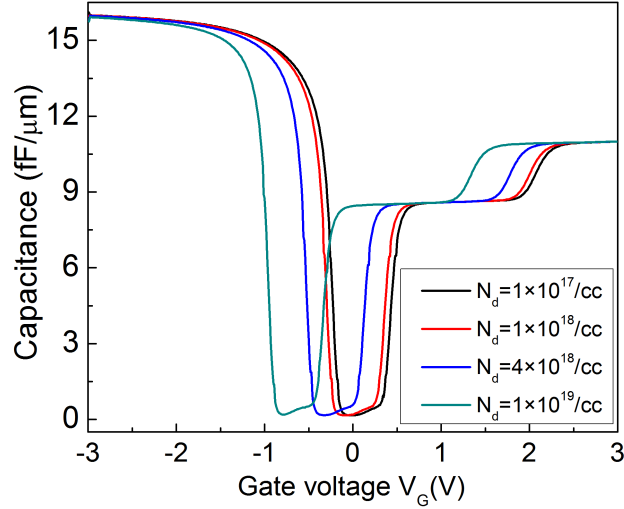
FIGURE 3.24: Effect of doping on CV curves of $In_{0.3}Ga_{0.7}$Sb XOI FET.

To investigate the compositional dependence of threshold voltage, FIG. 3.23 is presented. The threshold voltage increases from 0.335 V to 0.355 V for Ga composition from 0.5 to 0.7. Thus the composition dependent CV curves shown in FIG. 3.21 seem to be overlapped due to the small change in threshold voltage (20 mV).

3.2.3 Effect of doping

Figure. 3.24 shows CV characteristics as a function of doping concentration in the channel. The CV curves shift toward left (from positive to negative gate bias) with increasing doping concentration. Thus the threshold voltage of the device can be controlled by changing doping concentration. The doping concentration-dependent shift in threshold voltage implies that the device will no longer be enhancement type at high doping level. Also higher level of doping may reduce the carrier mobility by enhancing carrier scattering in the channel, and hence the device operation speed deteriorates. It means to ensure enhancement mode as well as high speed operation, doping level should be less than 1×0^{18}/cm3. It is also revealed that, the value of capacitance is independent of doping concentration at 1st and 2nd step CCRs.

To explain the CV characteristics in FIG 3.24, the band diagram along with 1st and 2nd eigen levels are shown in FIG 3.25 for different doping concentration and V_G=3 V. It shows both 1st and 2nd eigen levels get lower with increasing doping concentration.

As a result, less amount of gate voltage is necessary to populate them. This explains the left shift of the CV curves. But, once the 1st eigen is populated, the large difference between 1st and 2nd eigen and the lower density of states of III-V materials gives narrow room for further carrier increment, causing the capacitance to be constant (1st step CCR). Figure 3.26 shows that the threshold voltage decreases linearly with increasing the concentration of doping. It
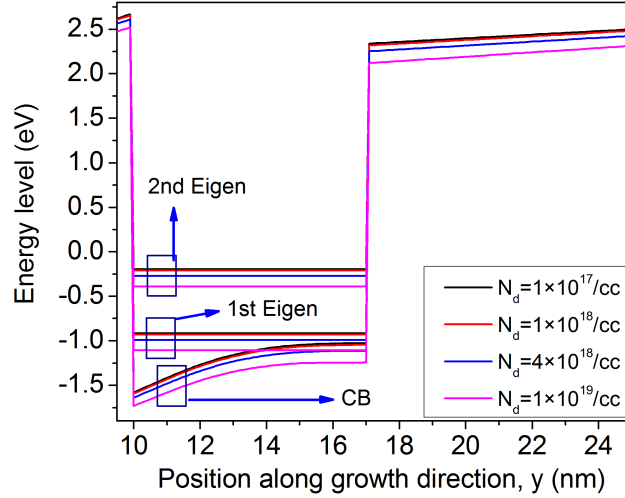
FIGURE 3.25: Doping concentration dependent Band diagram along with 1st and 2nd eigen energy of the device. The positions in the figures are measured from the gate-oxide interface along y direction as shown in FIG. 2.1.
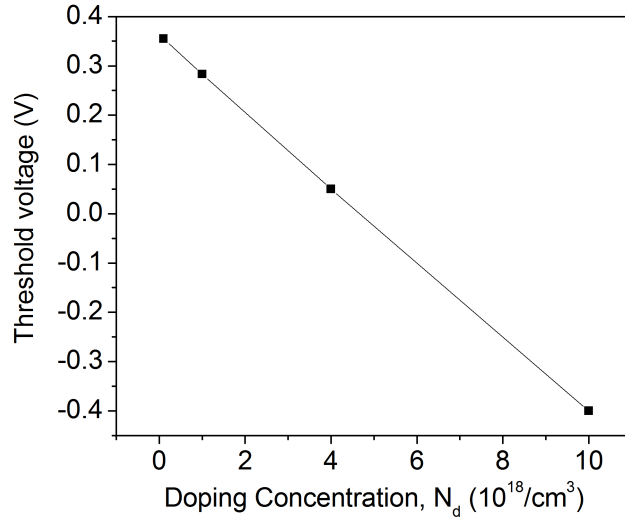

FIGURE 3.26: Threshold voltage of XOI FET as a function of doping concentration.

also reveals that for enhancement mode operation, that is for V_T to be positive, the doping concentration should be less than $4.67 \times 1018/\text{cm}^3$.

3.2.4 Effect of temperature

Effect of temperature on the CV characteristics is shown in FIG. 3.27. It is observed that the capacitance in each CCR is independent of temperature, T; but the slope of the transition from the minimum point to 1st step CCR and so from 1st to 2nd step gets steeper with decreasing T. It leads to have sharp control of turn on characteristics, and hence better subthreshold slope.

Figure 3.28 shows the conduction band profile, and 1st and 2nd eigen energy levels of the XOI FET. The results are obtained at $V_G=3$ V for different temperatures. It is observed that there is almost no effect of temperature on the energy bands and eigen levels. Also the separation
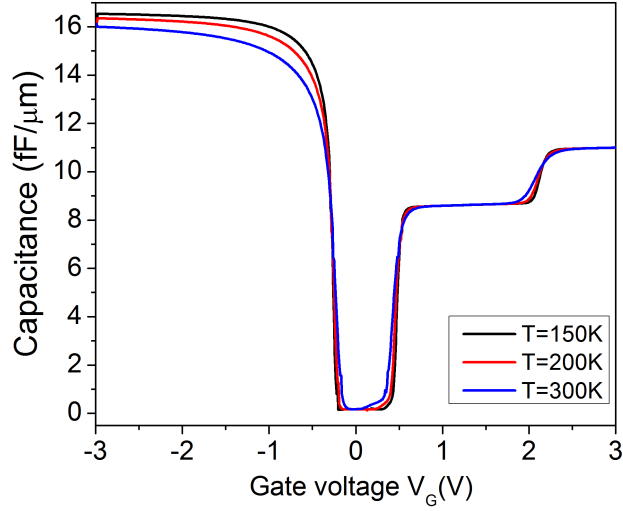
FIGURE 3.27: Temperature dependant CV profile of In0.3Ga0.7Sb XOI FET.
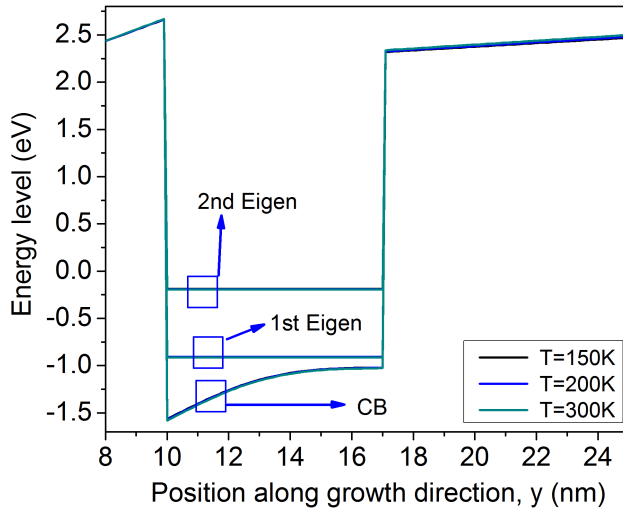
FIGURE 3.28: Temperature dependent band diagram along with 1st and 2nd eigen energy of the device.

between successive energy levels is high (greater than 0.69 eV) in comparison with thermal voltage, which is 0.026 V at room temperature. So at this temperature, thermal voltage can shift the band by 0.026 eV causing no effects in the capacitance at any CCR. But when Fermi level is very close to one eigen level, thermal voltage, or the temperature can affect the carrier

increment. This attributes the temperature dependent change in threshold voltage. FIG. 3.29 shows that the threshold voltage of the device decreases linearly with increasing temperature. The change in threshold voltage is found to be 81 mV for temperature change from 150 K to 300 K.
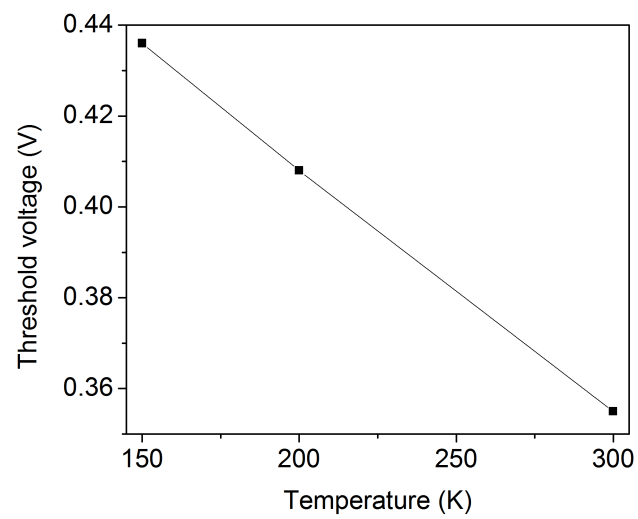
FIGURE 3.29: Temperature dependent threshold voltage of the XOI FET under study.

Chapter 4

Conclusion

Chapter Outlines

- Conclusion

- Recommendation for future work

4.1   Conclusion

In this study, the prospect of 15 nm gate length XOI FET for next generation ultra-low-power logic is studied. Several research work has been done for long channel XOI FET in the past in which carrier transport is diffusive, i.e., dominated by different scattering processes. But at sub 20 nm gate length, the transport becomes purely ballistic. Therefore results of the study on long channel XOI FET is not valid in this regime. That is why a full quantum mechanical transport study has been performed using widely used non-equilibrium Greens function theory.

It is observed that thinner channel performs better. But when the channel gets too thin, interface states as well as roughness start to dominate the device performance. However, impact of interface states can be compensated by engineering the gate metal work function. For long channel length of nFET, InAsSb is better as channel material because of its high electron mobility. But at ballistic regime, InGaSb outperforms InAsSb in all aspects of logic figure of merit. It is also observed that different gate oxide (HfO_2 and Al_2O_3) offers different device performance due to the difference in band offset with channel material, despite of same "Equivalent Oxide Thickness". However, the interface of the channel with these oxides should possess high quality and it greatly depends on process and passivation technology.

Capacitance-Voltage characteristic of the XOI FET, which is widely used to examine the quality of interface, is found to be different from traditional FET devices. It shows a staircase behavior when channel thickness becomes less than 15 nm. Above this thickness, the CV characteristics resembles to that of traditional FET devices. Doping concentration does not perturb the staircase behavior while affects the threshold voltage. However, temperature has negligibly small impact on the CV characteristic as well as the threshold voltage.

4.2   Recommendation of future work

In this study we kept the gate length of InGaSb XOI FET fixed to 15 nm. The future research related to this work can be carried out as:

- The effect of gate length scaling of XOI FET.

- Prospect of other emerging, specially 2D material like BN at the channel.

- Effect of using Schottky Source/Drain contact on the device performance.

- Full atomistic tight-binding study of the device performance.

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Journals:

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1. Md. Nur Kutubul Alam, Muhammad Shaffatul Islam, Md. Golam Kibria, Md. Rafiqul Islam, "Anomalous Staircase CV Characteristics of InGaSb-on-Insulator FET", IEEE Transaction on Electron Devices, Vol. 61, Issue. 11, November 2014.

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1. Md. Nur Kutubul Alam, Muhammad Shaffatul Islam, Md. Rafiqul Islam, "Ballistic performance comparison of III-V XOI and Junction-less XOI nFETs", 6th IEEE International Nanoelectronics Conference (INEC 2014), Hokkaido Univ., Sapporo, Japan. (In press)

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